DEVELOPMENT OF A SUBSTRATE CONFIGURATION CdTe/CdS SOLAR CELL ON FLEXIBLE MOLYBDENUM SUBSTRATE

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ABSTRACT

CdTe is one of the leading thin film photovoltaic materials with an optimum band gap of 1.5eV for the efficient photo conversion. The development of photovoltaic devices on metallic substrates is interesting due to the flexible nature of the devices. One of the hurdles in the development of CdTe devices on metallic substrates is that most of the metal foils do not form an ohmic contact with CdTe. We have used Au and Pd as the interlayer. The CdTe film was deposited onto the interlayer by close spaced sublimation. The CdS window layer was deposited by chemical bath deposition onto the CdTe surface and the devices were completed by sputter depositing In: SnO_2. We have studied the effect of post formation annealing treatments of the CdTe/CdS junction on the opto-electronic parameters of the device and correlated the opto-electronic properties with the inter-diffusion of Te and S across the CdTe/CdS interface. It was observed that the devices annealed at 400 °C show better photo voltaic properties. The AUGER depth profile analysis of the CdTe/CdS interface showed that the inter diffusion of Te and S increases with annealing temperature.

INTRODUCTION

The solar cells on flexible metallic substrates are light weight, free of damage and are suitable for space as well as terrestrial applications. For terrestrial applications, cells mounted on flexible foil have a special advantage since they can be wrapped onto any suitably oriented structure and the cost of support can be minimized. There are recent reports about the development of CdTe solar cells on flexible metallic and polymer substrates [1, 2]. CdTe is one of the leading thin film photovoltaic materials and is highly attractive due to high optical absorption coefficient, direct band gap of 1.5 eV and the variety of thin film preparation methods. We have earlier reported a 3.5% efficiency CdTe/CdS solar cell on flexible molybdenum substrate [3]. In this report we are discussing the development of the CdTe/CdS device on flexible molybdenum (Mo) substrate, the effect of post formation annealing of the CdTe/CdS junction on the inter-diffusion of Te and S across the interface and the opto-electronic properties of the device.

EXPERIMENTAL

The CdTe thin films were developed on flexible Mo substrates by CSS, Mo is considered as the suitable substrate material from the point of view of the matching thermal expansion coefficient with CdTe. But the difference in work functions of p-CdTe and Mo necessitates the need of an interlayer between CdTe and Mo substrate which can form a non-rectifying and low resistive contact between CdTe and Mo. We have used Au and Pd as the interlayer, a thin layer of (15 to 20 nm) Au or Pd was deposited on the clean Mo surface by sputtering. The CdTe films were prepared at substrate temperatures in the range 500 to 570°C and source temperatures of 550 to 650°C. Thin CdTe films of approximately 8 μm thickness were deposited onto the interlayer in four to five minutes. CdTe/CdS junctions were prepared by depositing approximately 0.1 μm thick CdS layer onto the CdTe substrates by chemical bath deposition (CBD) [4]. The CdTe/CdS devices were annealed at different temperatures in air and later the top contacting material was made by sputter depositing ITO on the annealed CdTe/CdS surface.

RESULTS AND DISCUSSION

The as deposited CdTe films were characterized using XRD, SEM and AUGER techniques. The films were polycrystalline with no preferred orientation for the grain growth. The average size of the crystallites was in the range of 1 – 2 μm. The composition of the film is uniform throughout the thickness of the film. The AUGER depth profile analysis revealed that the percentage composition of the film is 50.5% Te and 49.5% Cd.

The AUGER depth profile of the untreated CdTe/CdS device is shown in Fig. 1, the intermixing of the CdTe and CdS occurs in a region of approximately 0.2μm wide, which can be considered as the width of the interface. Beyond 0.4μm depth there is presence of sulfur (S) in the CdTe layer, which was diffused during the deposition of CdS from the chemical bath at 90 °C.

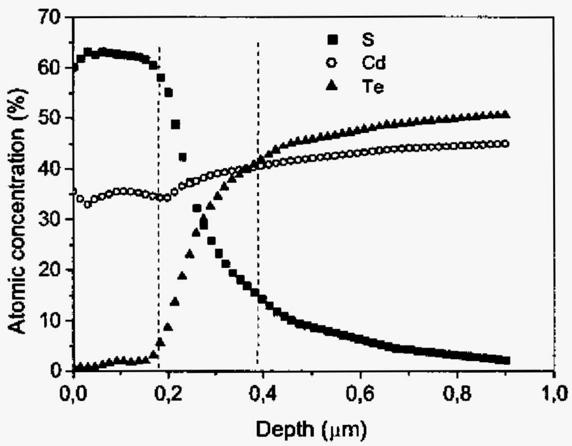

Fig. 1. AUGER depth profile of the as deposited CdTe/CdS device. The dotted lines show the width of the interface region.

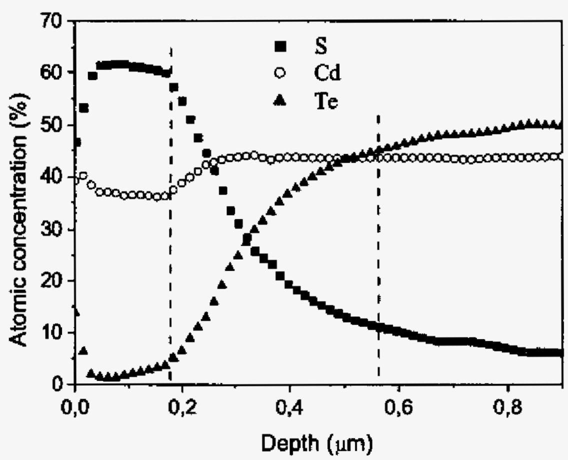

Fig. 2. AUGER depth profile of the CdTe/CdS device annealed at 380 °C. The dotted lines show the width of the interface region.

The AUGER profile of the CdTe/CdS device annealed at 380 °C is shown in Fig. 2. One can observe that the annealing causes inter-diffusion of both Te and S as well as sublimation of S from the CdS film reducing the effective thickness of the CdS layer. The width of the interface is more than that of the untreated device.

In the case of devices annealed at higher temperatures, the width of the interface region increases further (Fig. 3) and the thickness of the window layer decreases and finally disappears leaving a Cd rich $CdTe_{1-x}S_x$ surface. It was observed that the devices annealed at 400 °C shows maximum values for the open circuit voltage and short circuit current density and for higher annealing temperatures the devices show poor performance, indicating degradation of the device. This degradation can be due to the change in junction characteristics as well as due to the loss of CdS material from the surface. Annealing has two effects on the CdS layer; S diffuses into the bulk of the CdTe and also there is a loss of S from the CdS surface due to sublimation leaving a Cd rich surface. The observed improvement of the photovoltaic parameters at lower annealing temperatures can be due to the improvement of the CdS layer, passivation of defects as well as the improved junction properties and the reduction in lattice mismatch between CdTe and CdS due to inter-diffusion of S and T and the formation of $CdTe_{1-x}S_x$ [5]. Fig. 4 shows the relation between the calculated band gap of the CdTe and the annealing temperature of the CdTe/CdS device. The band gap was estimated from the photo current data of the device. The change in the band gap is considered as due to the formation of the alloy $CdTe_{1-x}S_x$.

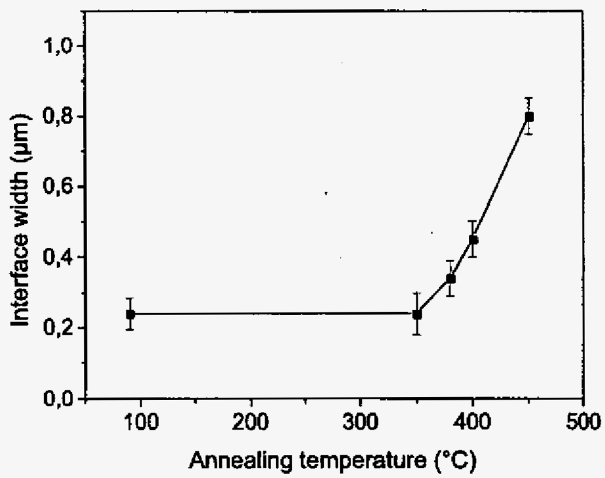

Fig.3. Dependence of the interface width on the annealing temperature of the CdTe/CdS device. The data was generated from AUGER depth profile analysis.

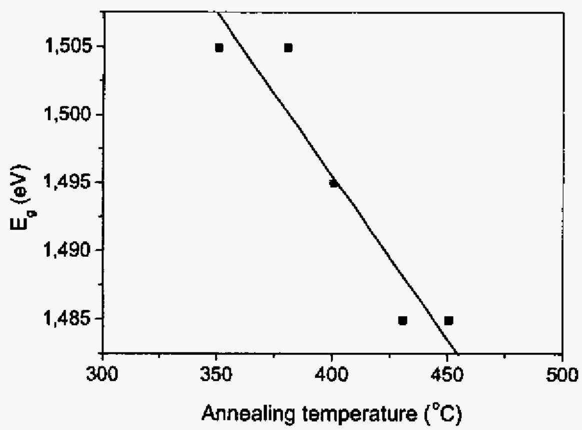

Fig.4. Relation between the measured band gap of the CdTe and the annealing temperature of the CdTe/CdS device.

CONCLUSIONS

We have developed CdTe/CdS solar cell on flexible molybdenum substrates. The dependence of the optoelectronic parameters of the cell on the annealing temperature of the CdTe/CdS device has been investigated and found that annealing at 400 °C results in better devices. The inter-diffusion of Te and S across the CdTe/CdS interface has been investigated. Work is in progress to investigate the effect of annealing and the thickness of the CdS layer on the efficiency of the CdTe/CdS solar cells.

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