2nd International Conference on Electrical and Electronics Engineering (ICEEE) and XI Conference on Electrical Engineering (CIE 2005)
Mexico City, Mexico. September 7-9, 2005

Charging/discharging effects in nc-Si/SiO_2 superlattice prepared by LPCVD

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Abstract — **Clear charging/discharging effects were observed in nc-Si/SiO_2 superlattice structures fabricated by LPCVD (Low Pressure Chemical Vapor Deposition). I-V measurements were performed at different voltage sweep ranges, voltage steps and delay times (which result in different voltage sweep rate). It was found that a clear current bump, which has a strong dependency on the measurement parameters, could be observed. This current bump is ascribed to the charging of the nc-Si dots in the superlattice structures. A new memory device based on this structure can be possibly developed.**

Keywords —**superlattice, charging, tunneling**

I. Introduction

A superlattice (SL) is a multilayer structure that could be represented by an array of multiple quantum wells, but with very thin potential barriers. As the thickness of the barriers is shorter than the electron mean free path, a tunneling across the barriers can occur if an allowed energy state of one side of the barrier is aligned with one of the other side. It is also expected a series of narrowed allowed and forbidden bands, due to a subdivision of the original Brillouin zone into a series of mini-zones [1]. Charging is allowed in the supperlattices at voltages out of the resonance condition because of the quantized states of the wells (nanocrystals or nanolayers) [2].

There are a number of reports about nc-Si/SiO_2 superlattices that looks to be compatible with the fabrication process of CIs. Most of the works use PECVD (Plasma Enhanced Chemical Vapor Deposition) and magnetron sputtering [3-7], and just some have been fabricated by epitaxial growth [8]. However, there are no reports of superlattices prepared by LPCVD; a few works present MOS like structures with embedded nanocrystals, but not superlattices [2, 9]. LPCVD is a very simple and conventional method of deposition, and has some advantages, as a simple way to vary the silicon content in an ample range.

Charging/discharging effects are very important for the development of new devices as floating point memories [2] and floating gate transistors. In this work, we will report our experimental characterization of charging/discharging effects in nc-Si/SiO_2 superlattice fabricated by LPCVD.

II. Experimental

A. Fabrication

The nc-Si/SiO_2 superlattices were deposited on n-type (100) Si wafers with resistivity of 2-5 Ωcm by LPCVD, followed by a high temperature thermal annealing (1100ºC during 2 hrs in N_2 ambient). The superlattice consists of 16 SiO_2 layers and 15 Si layers deposited alternately. The thickness of both the barrier (SiO_2) and well (Si) layers were varied, producing three different superlattices, as listed in Table I. The formation of the superlattices was corroborated by AFM measurements.

Thermal annealing at 1100ºC ensures the nucleation of the Si layers. The grain size is controlled by the layer thickness [3-7], therefore nanosized Si dots are formed in the well layers.

Aluminum was evaporated on both surfaces of the samples. The gate electrodes were patterned by standard photolithography. A schematic structure of the superlattice is shown in Fig.1.

B. Measuring methods

The current vs. voltage (I-V) measurements were done using a HP semiconductor parameter analyzer 4145A at room temperature. All the measurements were performed in a screening box in dark. The voltage sweep parameters were changed in order to investigate their influence on the I-V performance.

The I-V measurements were performed at different delay times (td), step voltages (Vstep), holding times (th) and voltage ranges (Vrange). When the delay time was set to 0 s, there was an intrinsic time between voltage steps, of 44 ms (40 ms of integration time -ti- and 4 ms of transition time -tt-). A scheme defining these parameters can be seen in fig.2.

TABLE I
LIST OF SAMPLES USED IN THIS WORK

Sample	SiO_2 thickness (nm)	nc-Si thickness (nm)	Total superlattice thickness (nm)
A	0.92	5	89.72
B	2.7	5	118.2
C	2.7	2.5	80.7

IEEE Catalog Number: 05EX1097
ISBN: 0-7803-9230-2
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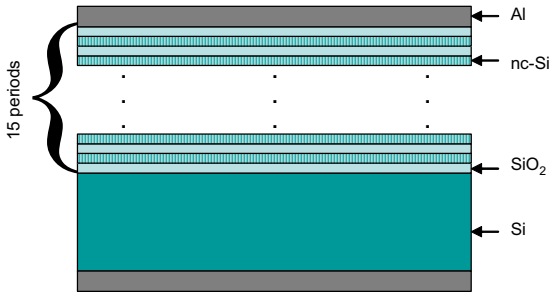

Fig.1. Schematic structure of nc-Si/SiO_2 superlattice

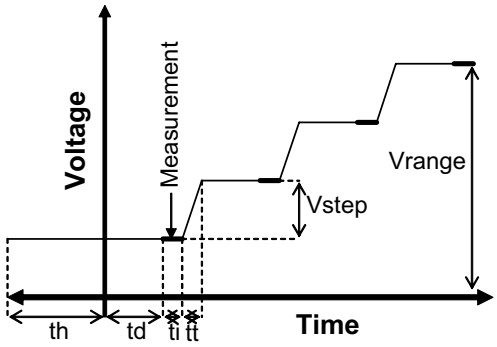

Fig.2. Scheme of the parameters in an I-V measurement

III. Results

From the I-V characteristics shown in Fig.3, it was found a positive current bump at -1.1V when the voltage was swept forwardly, that is when the applied voltage in the gate electrode started from negative towards positive values. This bump was found mounted over a "base current" caused by the charging of the electrode plates of the structure. Considering the whole structure as a capacitor, the base current can be visualized as the displacement current of this capacitor. The point where the current peak appears is called "point x", being used as a reference for comparisons between different measurements.

Measuring with different Vsteps, it was seen that the amplitude of the peak increases as Vstep increases, as shown in Fig.3, where I-V curves were plotted for a range of Vsteps from 5mV to 35mV. On the contrary, when the delay time is increased, the current bump decreases. This is notably observed in Fig.4, where there are plotted two I-V curves measured with different delay time (td = 0 s and td = 0.5 s). It can be found that the peak current amplitude reduces almost 5 times when the delay time increases from 0 s to 0.5 s.

It was also seen that if the voltage sweep is started from a more negative voltage, maintaining the same Vstep and td, the current bump increases having an almost linear relation with the magnitude of the negative voltage; this can be observed in Fig.5.

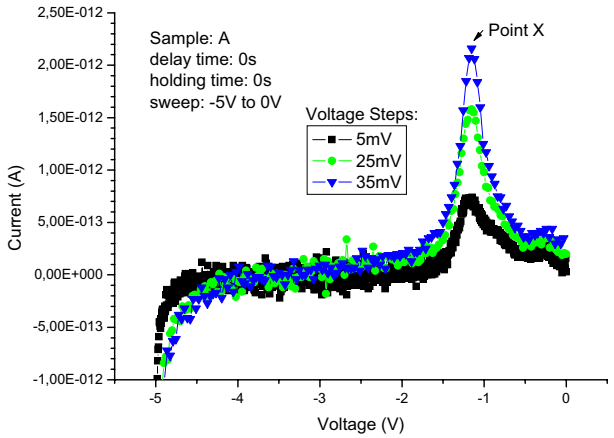

Fig.3. I-V plots varying the Vstep

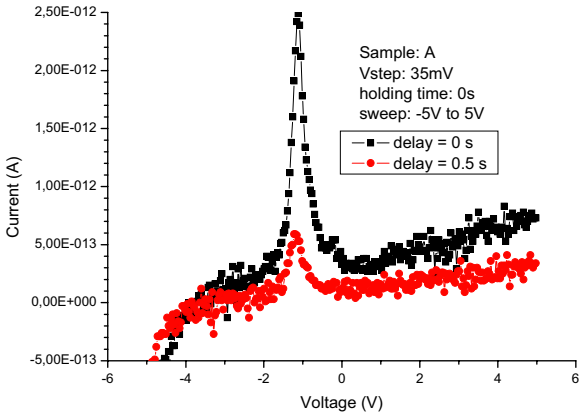

Fig.4. I-V plots varying the delay time

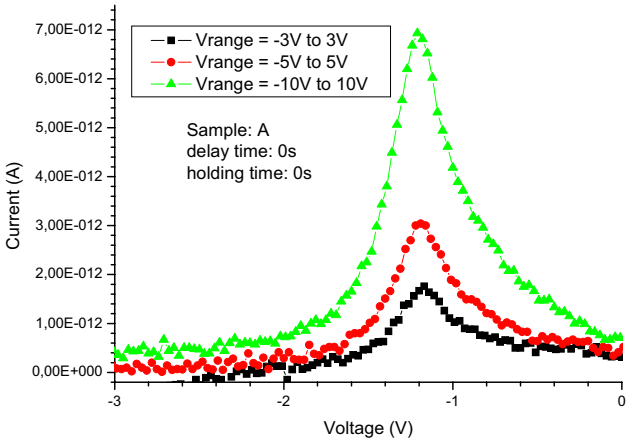

Fig.5. I-V plots varying the voltage range

IEEE Catalog Number: 05EX1097
ISBN: 0-7803-9230-2

IV. Discussion

When the structure is in contact with the voltage source for the first time, the structure tries to reach the voltage of the source. If the voltage sweep starts from a negative voltage, there is an electron current flowing from the source to the gate until the structure reaches the same voltage as the source (when there is no more charge transfer and the current is equal to zero); after this point, the voltage source has a more "positive" voltage than the structure, because the source voltage is moving toward zero; then the electron current flows from the gate to the voltage source, producing a positive current. In the I-V plots it can be seen that the current is always increasing, that is because the structure never reaches the increment of voltage Vstep in each step (the source voltage changes are faster than the velocity of charging of the electrode plates of the structure). At each increment of voltage, the difference in voltage between the source and the structure is increased, resulting in a greater current. This increasing current is called "base current", on which the current bump at point x is mounted.

If the structure is in the threshold voltage condition (where the current bump appears), energy levels of the first well (Si layer) of the gate side align with the Fermi level of the gate; when this happen, the stored electrons in the well are allowed to tunnel through the first barrier and reach the gate electrode, producing an extra current with positive direction mounted on the base current (the current bump at point X). Because this charge transfer process can only happen in the specific voltage where resonant tunneling across the first barrier can occur (-1.6V), therefore, the current reduces rapidly to the base current after this threshold voltage. The grain size in the well layer has a distribution, resulting in a wide current bump instead of a sharp current peak. The Gaussian-like shape of the current bump is probably the result of the Gaussian distribution of the grain size.

The released electrons by the well at the threshold voltage are the ones that are stored previously during the start of the voltage sweep. The amount of transferred charge to the well is proportional to the starting voltage because the available charge to be transferred depends directly on the applied voltage during the first steps; this can be seen in Fig.6, where a linear relation is observed between the peak current and the starting voltage.

The increase in the current when the Vstep is increased is due to a displacement current. Increasing Vstep means to increase the voltage sweep rate ($\Delta V/\Delta t$), because the time taken to have a voltage change is always the same (4ms of transition time, what is a characteristic of the equipment). The displacement current is a direct function of the sweep rate as described by (1).

$$i = C\frac{dV}{dt} \tag{1}$$

Fig.7 shows the peak current behavior of the superlattice depending on Vstep. A linear relation is found between the peak current and the sweep rate, which means that the capacitance is constant; this behavior shows that there is constant charge transfer for different Vsteps. The described effect evidences that the current bump is ascribed to the charge transfer between the gate and the wells.

When the delay time was increased, the current peak decreased; this happen because the charging effect is a time dependant process, whose velocity is controlled by the time constant τ that depends of the capacitance and the series resistance of the structure. The current during the charging process can be represented by (2), where i_0 is the displacement current.

$$i = i_0 e^{-\frac{t}{\tau}} \tag{2}$$

From (2), it is expected an exponential behavior of the peak current at varying the delay time; this was corroborated in Fig.8, which is the plot of the peak current versus the delay time. It was found that the time constant for the charge transfer process is 0.14 s.

The same charge transfer behavior is presented in the samples B and C, as shown in Fig.9. However, the current magnitude varies according to the thicknesses of the sub-layers of the superlattice.

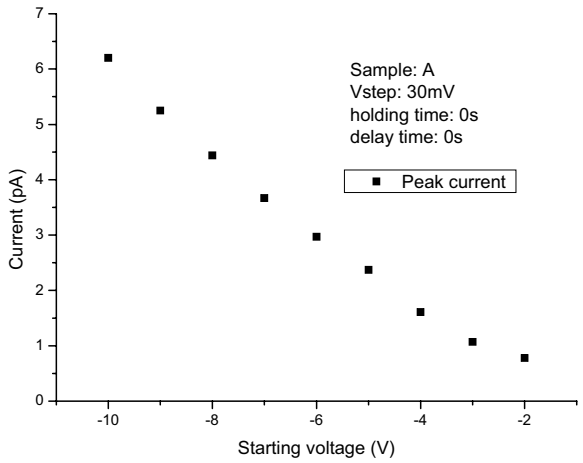

Fig.6. Plot of the current magnitude at "point x" for different starting voltages.

IEEE Catalog Number: 05EX1097
ISBN: 0-7803-9230-2

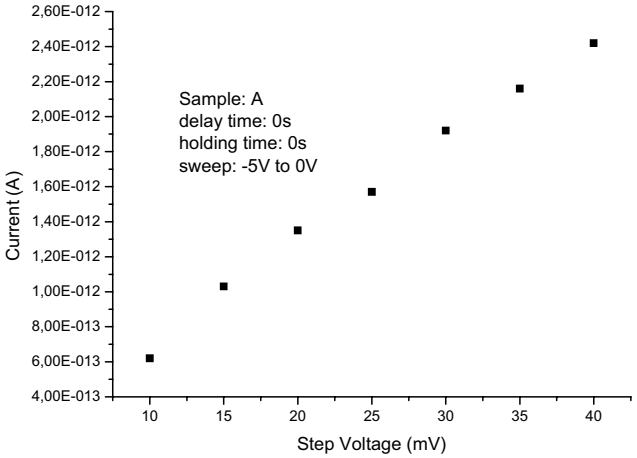

Fig.7. Plot of the current magnitude at "point x" for different Vsteps.

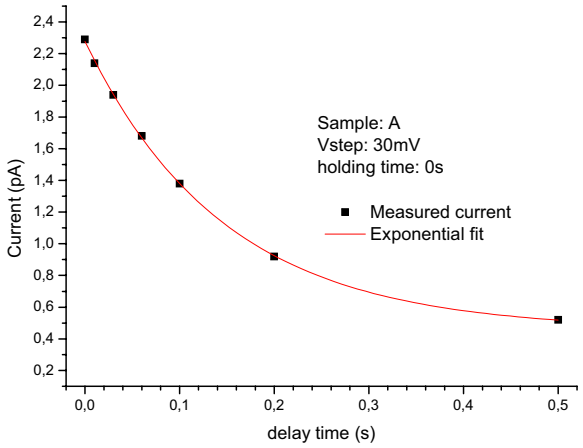

Fig.8. Plot of the current magnitude at "point x" varying the dalay time.

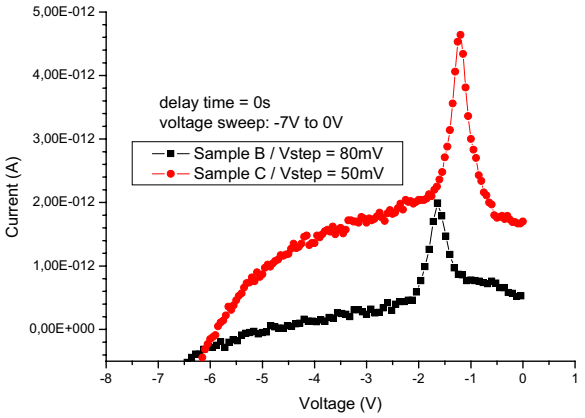

Fig.9. Plot of the I-V curves of samples B and C

V. Conclusion

It has been demonstrated that the superlattice structure fabricated by LPCVD presents clear charging/discharging effects. These effects are due to charge transferring between the gate contact and the subjacent Silicon wells.

The increase and the decrease of the current bump magnitude by increasing Vsteps and delay times respectively are caused by a displacement current, and it does not contribute to the amount of stored/released charge. The amount of charge in the structure depends of the voltage range used and the thickness of the layers.

Acknowledgment

The authors want to thank to the Microelectronic Lab technicians, especially to Mauro Landa, Pablo Alarcón and Ignacio Juárez for their support in the preparation and measurement of the samples. We also appreciate the support of CONACyT.

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IEEE Catalog Number: 05EX1097
ISBN: 0-7803-9230-2