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How to Make Optimized Arrays of Si Wires Suitable as Superior Anode for Li-Ion Batteries

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The fabrication process to produce Si wires with superior structural properties for application in Li-ion batteries is described. The process is based on the electrochemical etching of pores in Si, followed by a chemical over-etching step. The wires obtained have a quadratic cross section of around 1.5 × 1.5 μm and are organized in an array stabilized by two in-situ-created supports. An electrodeposited Cu film on the array is used as current collector. The method described is a production-near process with a potential for low costs and high yield.
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The maximum capacity of the present state-of-the-art graphite anodes is about of 370 mAh/g, but in practice this number is somewhat lower and found in the 330 mAh/g range.[1] Si, on the other hand, has a nominal anode capacity of 4200 mAh/g, more than ten-fold that of standard graphite anodes.[2] Additionally, the potential difference of Si *vs* Li/Li^+ is only about 0.5 V and thus not much more than the standard graphite anodes. The voltage difference between a lithiated and a delithiated anode is then around 0.5 V. Despite these obvious advantages, Si in its bulk state is useless as an anode, because the incorporation of Li leads to a volume expansion of up to a factor of 4, and the resulting stress fractures the material into dust rather sooner than later during cycling.

Nanostructuring Si has been thought as a solution to overcome the problems caused by volume expansion. One of the most promising solutions is the use of Si nanowire arrays.[1] Si nanowires, while still increasing their volume fourfold (mainly by doubling their diameters) during the incorporation of Li, do not fracture if they are thin enough. Some random arrangement of nanowires, with a diameter distribution centered on 90 nm, were tested in[1]; it was found that they could withstand more than 10 charging / discharging cycles without significant loss of capacity. Nevertheless these wires could have some problems upon prolonged cycling. In this way different strategies have been tested to improve the cycling performance of nanostructured Si-based anodes, for example, by improving their conductivity. Some examples of these attempts are, among others, thin layers of amorphous Si deposited on carbon nanofibers (electrical conductors),[3,4] mixing Si particles with conducting materials,[5] and mixing "wires" with carbon-based additives.[6,7] Another drawback of most Si nanowire anodes at present is the high cost of most of the actual fabrication techniques, which are not suitable for mass production. In our group a new fabrication technique that can be scaled up for mass production has been developed.[8–11] In this paper details of the process are presented.

For the production of Si wire anodes three major techniques are used at present:

1. Standard vapor-liquid-solid (VLS) technique, using mostly "Au droplets" as catalytic growth sites.[1,12–14] The wires are mostly grown on a current collector, mainly stainless steel.
2. Metal-assisted catalytic etching of single-crystalline silicon.[15,16]
3. Electrochemical macropore etching followed by chemical over-etching (our technique; discussed in detail later). The wires are then contacted to a Cu current collector by electrochemical means.

The first two methods must expect problems with respect to performance and mass production. These methods usually produce a random array of wires with different sizes and shapes. This does not allow optimizing the packing factor P (ratio of Si wire volume / total volume) without using more complex processes like sub-μm lithography.[17,18] The limit $P \leq 0.25$ obtains since there must be enough free space to allow the volume expansion, but smaller values produce less than optimal capacity.

Mass production requires low costs and at least method 1 will run into difficulties here. Since the weight of an anode comprises the weight of the Si plus the weight of current collector and supporting structures, optimized anode geometries call not only for $P \approx 0.25$ but also for large aspect ratios (wire length / diameter) of the wires, which must be obtained in a reasonable time. However, for large aspect ratios the wires tend to collapse and stick to each other. This stiction effect is an important drawback for method 2, since it makes it very difficult or rather impossible to contact the wires to a current collector.

The third method, the focus of this paper, does not suffer from the problems enumerated above as will become clear in what follows.

The Si wire anodes developed by our group can be described with the schema of Fig. 1. This structure has some advantages with respect to the wire arrays produced by other groups: (1) First, with the in-situ production of supports the stiction effect is avoided. (2) The free standing structure of wires with supports allows the electrochemical deposition of Cu on the surface of the array and also between wires until certain depth. This type of contact is mechanically stable. (3) The wire narrowing at the bottom makes the detaching of the wires from the substrate much easier; the Si substrate can be used for further production of wires.

The steps for the preparation of the wires described in Fig. 1 can be summarized in the following points:

a) Lithography and pre-structuring of Si wafers.
b) Electrochemical etching of macropores.
c) Chemical over-etching of macroporous Si.
d) Deposition of Cu current collector.
e) Detaching of the anode from the Si substrate.

The different steps will be discussed in detail in what follows.

Process

Lithography and pre-structuring of Si wafers.— The first step of the process is standard photolithography to define an array of dots where some holes will be etched. For the first tests the starting material has been 6″ p-type (100) Si wafers with resistivity 15–24 Ωcm with Al back contact. A positive photoresist is spin-coated on the wafers, obtaining a homogeneous film with a thickness of around 1 μm. For the lithography, a photomask with a quadratic array of circles of 1 μm in diameter and with 3 μm distance between the centers of the circles is used. After the exposure and development of the samples, wafers with a regular array of holes in the photoresist are obtained.

The structure is first transferred into the Si by reactive ion etching (RIE). The etching gases are SF_6 and Ar in a proportion 5.5 : 7 sccm, and the used power is 300 W. An array of holes in Si with a depth

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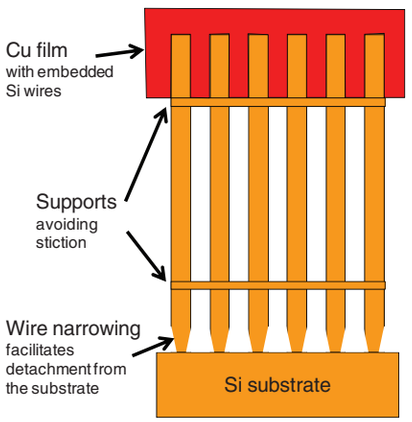


Figure 1. Schematic structure of the Si wire anodes prepared by electrochemical etching of pores in bulk Si.

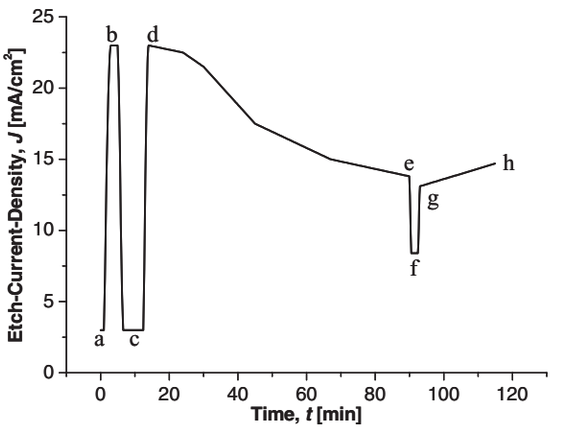
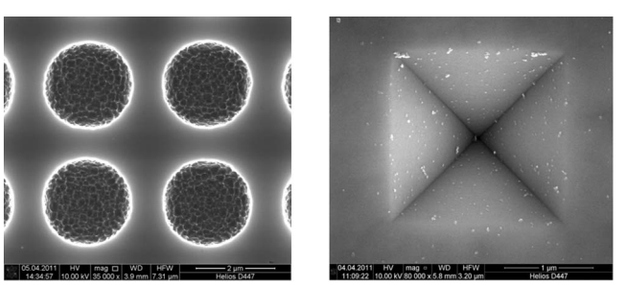


Figure 3. Current density profile for the macropores etching.

of around 2 μm is formed and most of the photoresist is removed as well. After a cleaning process in acetone under ultrasonication to remove the rests of photoresist, the samples look as observed in Fig. 2a. These structured samples have a very defined pattern, but they are still not useful for electrochemical pore etching, since the pores could still grow wild in any point of the wafers, by probability, as described by the current burst model.[19,20] It is then necessary to create peaky holes to define points where the growing of pores is more probable. For this purpose the samples are treated with a KOH solution to create inverted pyramids. The production of inverted pyramids is very well known by now but usually done by using a sacrificial masking layer like SiO_2 or Si_3N_4.[21–23] A process to etch without a "hard" masking layer has been developed for our purposes. The solution is composed of 100 mL of a 20 wt % aqueous solution of KOH and 0.5 g of polyethyleneglycol 3400. Etching for 45 min at 50°C produces hole shapes like the one shown in Fig. 2b. The etched samples are then useful for electrochemical pore etching.

Electrochemical etching of macropores.— The etching of the macropores with a special pore diameter – depth profile is one of the decisive factors for producing uniform and stable arrays of Si wires on a production scale. Although a lot of work has been done with respect to p-type silicon (pSi) macropore formation,[24–27] it takes tight parameter control and optimization to achieve the required structures. An organic electrolyte consisting of 5 wt % hydrofluoric acid (HF) in N,N- dimethylformamide (DMF) was used, and the temperature was kept constant at 20°C. The electrochemical etching process was done galvanostatically using the current profile as shown in Fig. 3. The whole etching process was done by using a complete etching system from ET & TE.[28]



(a) (b)

Figure 2. a) Structure transfer with RIE. The holes are around 2 μm deep. b) Inverted pyramid obtained after etching with the KOH-based solution developed.

The need for optimizing the current density for the macropores formation can be clearly seen in Fig. 3, i.e., the used current profile is not simple. The procedure starts with a low current of 3 mA/cm^2 (Fig. 3, position a). This allows a very good nucleation process,[29] which is very important for stable macropore formation and avoidance of early destruction of the pore walls due to leakage current. But since time is very crucial for the complete process and it takes too long to etch with low current densities, the current density is then increased to the optimized value of 23 mA/cm^2 (Fig. 3, position b). This increment of the current also increases slightly the pore diameter. In order to provide for the first stabilizing layer it is necessary to reduce the current density for short time again (position c in Fig. 3). This decreases the pores diameter thereby increasing the size of the pore walls (Fig. 4, position a). This is a very important step because after the chemical over-etching of the pores to form the wires (explained in the next section), a continuous Si support layer is left between the wires, keeping them upright and avoiding sticking. This allows for an easy deposition of copper on top of the wires later. The same process but with different parameters is repeated after approximately 120 μm pore etching, (Fig. 3, position f, and Fig. 4, position b) so there will be two separate support layers fixing the position of all wires. It has to be mentioned that the ability to vary the pore diameter in shallow depths needs significant variation of the current density, while for deeper pores just a slight variation of the current density is enough. This is due to diffusion limitations of the electrolyte during the etching process, which determines the effective HF concentration

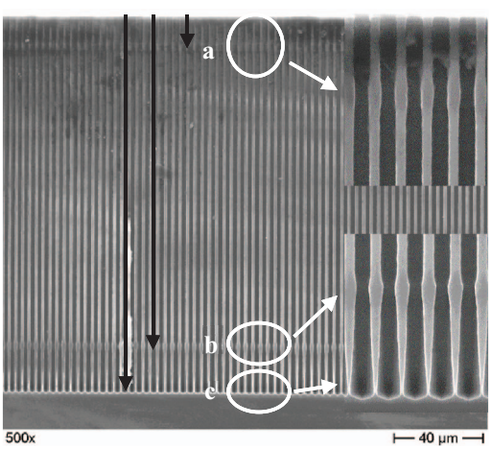


Figure 4. Resulting macropores with three diameter variations at different depths: a) ~ 10 μm, b) ~ 120 μm, and c) ~ 150 μm.

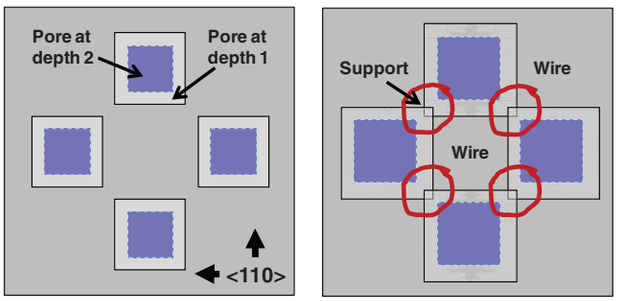


Figure 5. a) Schematic of the top view of the macropores. The pores have a cross section area of around 2 × 2 μm (pore at depth 1), but they are narrower at certain depth (pore at depth 2), where supports are created. b) Schematic of the pores after an anisotropical chemical etching process. The pores at depth 1 merge forming the wires, but at depth 2 the pore walls remain, which are the supports between wires.

at the tips.[29] Since the current density is proportional to the amount of positive charges (which is responsible for the etching of pores in general),[30] altering it has great influence on both the etch rate and the pore diameter. In this work, the choice of the electrolyte and Si material used ensures that altering the current density does not have great influence on the diameter of the less deep pores but rather on the etch rate. This phenomenon is completely the opposite for deep pores where a slight change in the current density has a huge influence on the pore diameter and nearly non on the etch rate.

The almost exponential decrease in the current density (Fig. 3, from position d to e) is necessary to keep the etch current at the pore tips constant with respect to the effective HF concentration.[30] Keeping the current density constant for the whole etching time for instance, will lead to cavity formation after some depth and a complete destruction of the pore array. This could happen because the rate of the oxide formation will be higher than its dissolution at the pore tips due to diffusion limitation of the electrolyte.[24]

The slight increase in the current density towards the end of the pore etching process (Fig. 3, from g to h) is to increase the diameter of the pores to create almost a "cavity" (Fig. 4, position c). This is of great importance, since the final goal is to detach the wires from the bulk material (as discussed in section 2.5).

Chemical over-etching of macroporous Si.— The pore diameters are increased by uniform chemical over-etching until pore walls touch and only the wires remain; this is accomplished with an anisotropical etching solution based on KOH at 50°C in 1.75 h. The etchant is composed of 100 mL of a 0.45 wt % aqueous solution of KOH and 2 g of polyethyleneglycol 3400. The "stopping planes" in Si for this solution are the (110) planes, thus the produced wires are (110) faceted. To understand the process a schematic is shown in Fig. 5. The starting macropores have the shape described in the last section; Fig. 5a shows a schematic of the top view of the pores. The pores have a cross section area of around 1.5 × 1.5 μm (pore at depth 1), but they are narrower at certain depth (pore at depth 2, Fig. 5a), where supports are created. Upon etching, the pores become wider, with walls faceted in the ⟨110⟩ orientation. Wires are formed when the pores merge, as indicated in Fig. 5b, but at the pore depth 2 walls remain acting as supporting planes. SEM images from the top view of macropores and particles are shown in Fig. 6a and 6b respectively. In Fig. 6b it is possible to observe the support between the wires.

An advantage of the etchant developed for this work is that it etches with almost the same rate at the full depth of the macropores; i.e. supplying a large process window (in contrast to standard acidic etches).[11] A side view of the produced wire array is shown in Fig. 7. Two supporting planes can be recognized, and it can be seen that at

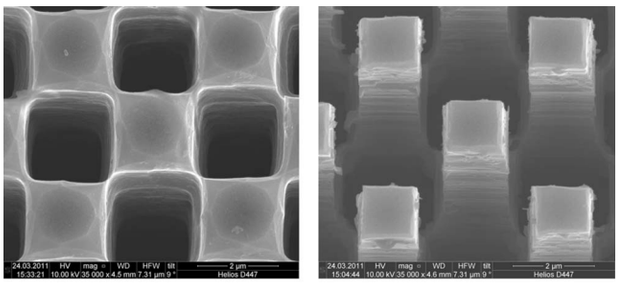


Figure 6. SEM images of the top view of a) macropores and b) wires. It is possible to observe the supporting layer between wires.

the bottom the wires are narrower; this is a result of the current profile chosen during the electrochemical pore etching.

Deposition of a Cu current collector.— While it would be easy to sputter Cu on top of the stabilized wire array, this would be an expensive process for a thickness of several μm. Also the adhesion of such a Cu film on Si would be poor. That is why it is common to use additional adhesion layers before the deposition of Cu, like TiN (which also works as barrier layer),[31] making the process costly. Secondly sputtering would not allow for an easy Cu deposition between wires (it is preferable to have the wires embedded in Cu to improve the mechanical contact). Therefore an electroless Cu seed layer deposition followed by regular galvanic deposition of several μm of Cu has been used. While Cu electroplating in general is a known process, direct electrochemical deposition of Cu over isolating wires (the Si wires behave as isolators in this process) is without precedent. A substantial amount of work was necessary to overcome the main problems for deposition of Cu over the wires.[11] The first step is chemical or electroless deposition of a seed Cu layer of around 100 nm. This is accomplished using an acidic solution, process that is not standard. As soon as the electroless deposited layer is thick enough so that a continuous Cu film exists connecting all wires by the uppermost supporting plane, the seed layer can be used as a conducting path for electroplating just by contacting it from the edges.

The solution for the chemical deposition is prepared with 2 mL HF 48%, 98 mL H_2O and 1.9 g $CuSO_4 \cdot 5H_2O$. The deposition is performed at 30°C within 5 min. There are some reports about electroless

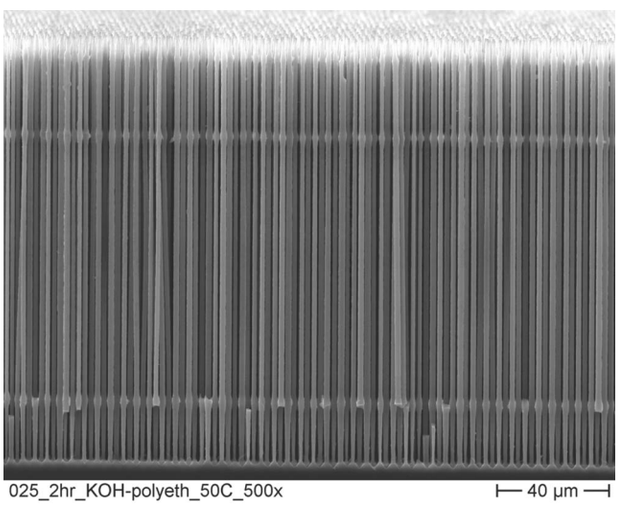


Figure 7. SEM side view of the Si wire array. Two supporting planes are visible.

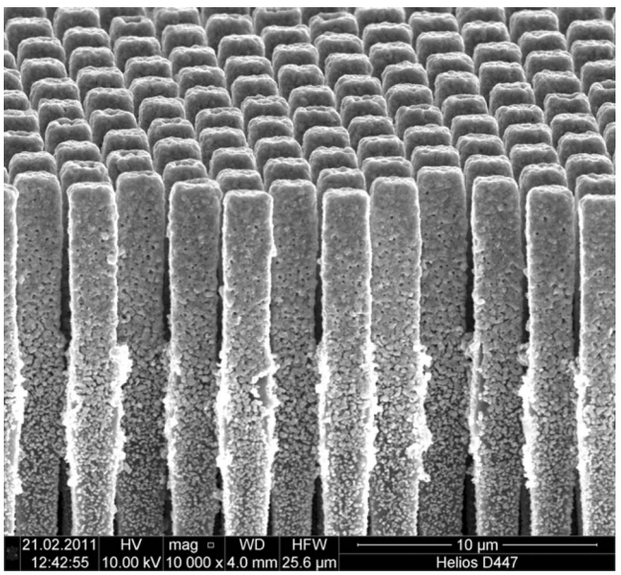


Figure 8. Si wires with an electroless deposited Cu layer.

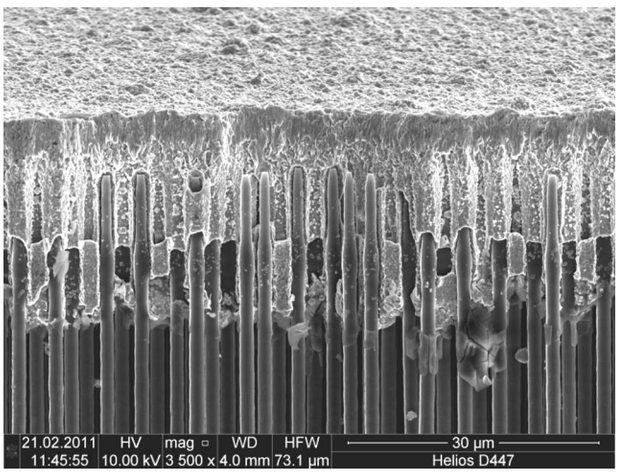


Figure 9. Si wires with an electrochemically deposited Cu layer.

deposition using an acidic solution based on HF, but in those cases Si is used as a sacrificial material.[31,32] Si reacts with HF releasing 4 electrons; these electrons are accepted by Cu^{2+} ions, leading to the direct Cu deposition on the Si surface. This redox process can be described by the following two half-cell reactions:

$$Si + 6F^- \rightarrow SiF_6^{2-} + 4e^- \quad [1]$$

$$2Cu^{2+} + 4e^- \rightarrow 2Cu \quad [2]$$

The deposition is accomplished until the desired depth by control of the concentration. If larger amounts of the reactants are used a deposition is just found on the top of the wires. The process was optimized for deposition into the depth of the first support layer as shown in Fig. 8.

After forming the Cu seed layer the electrochemical Cu deposition is performed using a solution composed of 2.5 g $CuSO_4$, 9.6 mL H_2SO_4, and 100 mL H_2O. The deposition is done with a constant current of 5 mA/cm^2 at 20°C. Up to now the electrochemical step takes a long time (10 h for 50 µm), but permits high quality Cu films with the desired thickness. A picture of Si wires with a finished Cu layer is given in Fig. 9.

Detaching of the anode from the Si substrate.— The last step consists of detaching the Cu-covered wires from the substrate. The Cu film of around 50 µm is mechanically stable and can be bent and pulled without braking. The Cu film is simply pulled from the substrate, and as the wires have a very good mechanical contact with it, they are also detached from the substrate. An example of a finished coin-size anode is shown in Fig. 10, but all production steps are scalable to full 6 inch wafer size.

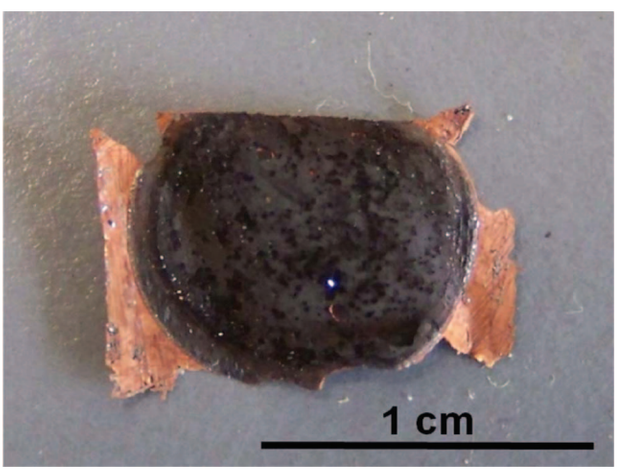


Figure 10. A finished coin-size anode of Si wires. The dark part of the center is the array of wires.

Cyclic Voltammetry

Cyclic voltammetry tests were performed with the anodes in order to identify redox processes. For this purpose, half-cells were prepared, with Li as reference electrode. The separator was a glass fiber fleece, and the electrolyte was LP-30 (0.5 ml), consisting of dimethylcarbonate and ethylencarbonate (1:1) plus 1 mol/l of $LiPF_6$. The experiment was performed for 60 cycles in the range of 0 to 1 V, at a voltage sweep rate of 0.1 mV/s. Selected voltammograms are shown in Fig. 11. As can be observed in the figure, the same peaks appear from

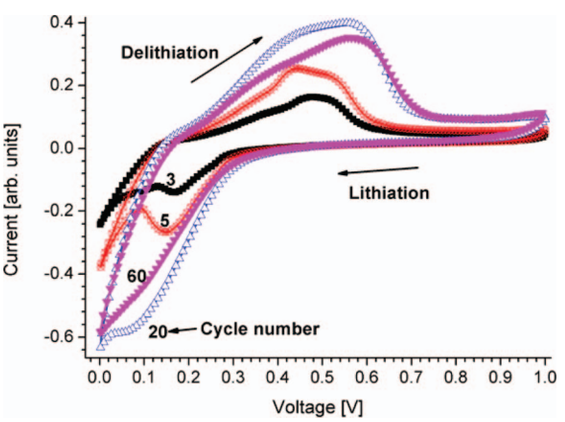


Figure 11. Selected cyclic voltammograms of the Si wires. The voltage sweep rate was 0.1 mV/s.

the first cycles until cycle 60, indicating that the same processes occur in all the cycles. During the lithiation (decreasing the applied voltage) two peaks appear (peaks 1 and 2); peak 1 upsets at 300 mV and the position of its maximum shifts to lower values upon cycling. Peak 2 starts at around 50 mV. During the delithiation process also two peaks appear (peaks 3 and 4). Peak 3, present as a shoulder, has a maximum at around 350 mV. The position of the maximum of Peak 4 shifts to higher values upon cycling; for example, it is at 475 mV for cycle 3, and at 565 mV for cycle 60. The positions of the peaks are consistent with different reports on Si anodes, with small variations due to the cycling rate, electrolyte, size of the Si wires, and effectiveness of the current collectors.[7,33–35] According to the TEM analysis reported in,[33] peak 1 could be attributed to the formation of polycrystalline $Li_{13}Si_4$, while peak 2 may represent the highest lithiated Li-Si phase, possibly $Li_{22}Si_5$. The delithiation peaks 3 and 4 could be attributed to $Li_{12}Si_7$ and poly or amorphous Si. The shifts of the peaks and their increase in intensity could be associated to the progressive "activation" of the wires in depth, due to the increasing breakdown of the crystalline silicon structure.[34] This experiment evidences that only Si-Li phases are formed upon lithiation/delithiation of the present wires, and that the wires stand 60 cycles without any problems.

Conclusion

A complete process for the production of anodes of Si wire arrays has been developed. The details of the process steps have been described. This method allows the preparation of very homogeneous arrays of wires in a simple and economical process. Voltammograms recorded for 60 cycles confirm the existence of only Li-Si phases in the wires upon lithiation/delithiation. The charging/discharging performance of Si anodes prepared by our group previous to this work is encouraging (see[8,11]); a complete analysis of the cycling performance of the present Si wires is also envisioned, and the results will be reported elsewhere.

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