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Optimized Cu-Contacted Si Nanowire Anodes for Li Ion Batteries Made in a Production Near Process

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Anodically etching macropores in Si substrates followed by chemical over-etching and Cu galvanics allows producing Si nanowire anodes for Li ion batteries with optimized geometry. This paper focuses on the optimizations of the process chain. The times for key processes could be substantially reduced while concomitantly improving the quality and the process window. The process chain now is close to enabling mass production on 200 mm wafers.
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The promise of affordable electrical cars in the near future can only be met if major progress will be made with respect to the Li ion battery performance. The energy per kg of present state-of-the-art Li ion batteries is at best around 2% of that of liquid fuel, and batteries with a substantially higher specific capacity are needed. The capacity of a Li ion battery is directly proportional to the amount of Li that can be intercalated into a weight unit of the anode (and cathode); it is typically expressed in mAh/g. Just as important for mass applications are specific costs expressed, e.g., in €/Wh.

In what follows only the anode of a Li ion battery will be considered. The maximum capacity of the present state-of-the-art graphite anodes is about of 370 mAh/g. In practice this number is somewhat lower and found in the 330 mAh/g range.[1]

It has been known for some time that Si would make a much better anode with a nominal anode capacity of 4200 mAh/g, more than ten-fold that of standard graphite anodes.[2] Just as important, most (>80%) of the Li can easily be taken out again, and a Si/Li anode just reduces the possible battery voltage by about 0.5 V upon discharging, thus not much more than the standard graphite anode. Despite these obvious advantages, bulk Si is useless as an anode, because the intercalation of Li leads to a volume expansion of up to a factor of 4, and the resulting stress will invariably fracture bulk Si into dust.

In a groundbreaking paper Chan et al. showed in 2008 that this problem could be overcome by using nano-structured Si in the form of nanowires.[1] Si nanowires, while doubling their diameters during the intercalation of Li, do not fracture if they are thin enough. Some random arrangements of nanowires, with a diameter distribution centered around 90 nm were tested in Ref. 1; it was found that they could withstand more than ten charging/discharging cycles without significant loss of capacity. Meanwhile, substantial progress has been made concerning nano-structured Si as anode material[1,3,6–8] and the viability of the approach is now beyond reasonable doubt. While large-scale tests in batteries are not yet available, all results obtained so far indicate that nano-structured Si might meet all battery requirements and thus might be found in commercial batteries of the near future.

The nanowires in most papers addressing this topic were grown with the standard vapor-liquid-solid (VLS) technique, using mostly "Au droplets" as catalytic growth sites,[1,7,9,10] or by metal-assisted catalytic etching of single-crystalline silicon.[5,11] This paper addresses an alternative way for producing suitable Si nanowire anodes. First the basic techniques for producing Si nanowire arrays with optimized geometry via macropore etching in Si and Cu galvanics will be briefly described. Next, relevant test results with these anodes tried in standard batteries will be presented. The main part of the paper then deals with the substantial improvement of the structure of the anodes concerning to the drawbacks observed in the previous results; the concomitant reduction of process costs by optimizing the process chain is also discussed.

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Basic Process for Producing Nanowire Anodes

Macropore etching and subsequent nanowire array production.— The basic procedure for making nanowire arrays consists of two processes: (i) anodically etching macropores into p-type (or n-type) Si wafers, and (ii) chemically over-etching the pores (i.e., increasing their diameters) until pore walls touch and only the interstices = nanowires are left, see Fig. 1a.

The first step is to produce arrays of nuclei for the subsequent macropore etching process by (cheap) standard contact lithography. The lattice type and lattice constant a of the array determines the distance between the nanowires and the "Si efficiency" SE, i.e. the ratio of the Si volume remaining in the nanowires to the Si volume removed. Knowing from experiments that the volume expansion of the Si nanowires is practically completely due to a change of their lateral dimensions (i.e. doubling of their diameter), the best possible Si efficiency value is $SE = 0.25$ since at least $^3/_4$ of the Si needs to be removed to allow for expansion in the lateral direction.

Etching Si macropores in arrays with lattice constants between about 0.5 and 10 μm is fairly routine by now, cf. Refs. 12 and 13 It can be done either in lightly doped n-type or p-type Si. For what follows, typically 1 cm^2 sized p-doped {100} Si with doping levels corresponding to a resistivity of 15–24 Ω cm was used. The electrolyte was typically HF 5 wt % diluted with DMF. Typical etching conditions were: temperature $T = 20°C$; current density $j = 3$–23 mA/cm^2, following some optimized function of time; total etching time around 110 min for pore depths around 150 μm. Etching equipment from ET&TE (Ref. 14) was used, details of the process are described elsewhere. The etching process was monitored and controlled in-situ by impedance spectroscopy, cf. Ref. 15.

Increasing the pore diameters by isotropic chemical over-etching using well-documented HF/HNO_3/HAc mixtures[16,17] is simple in principle but time consuming and difficult in reality (small process window). It can be done, however; more details are given in Sec. 4.

Isolating the substrate by a galvanically deposited Cu layer.—The nanowire structure shown in Fig. 1 cannot yet be used as a good anode because the Si substrate at the bottom of the nanowires will also incorporate some Li. Subsequent fracture destroys the structure within a few charge/discharge cycles. This can be avoided by depositing a several μm thick Cu layer (which is impervious to Li) on top of the substrate, effectively embedding the nanowires in an unyielding Cu layer that also thus provides the best possible electrical contact or current collector.

However, as found out in recent years,[18–22] Cu galvanics, while routinely used in metallurgy and Si microelectronics, is far from easy inside macropores and not yet well understood. This is also true for depositing Cu at the bottom of a nanowire array. While it

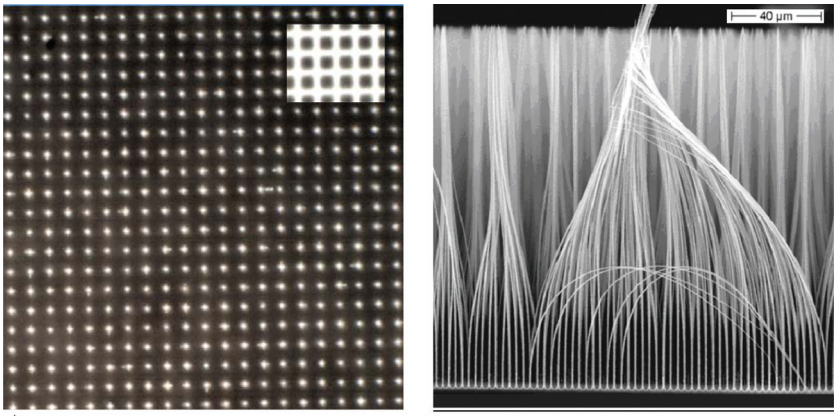


Figure 1. (Color online) (a) Top view of nanowire array; the lattice constant is 4 μm. The inset shows the macropores before over-etching. (b) Cross-section of ordered nanowire array: (b) Shows a cross-section of a nanowire array produced in this way. It also demonstrates two pertinent points: (i) the nanowires are very stable and not given to fracture when mechanically challenged; (ii) there is a tendency for "stiction," i.e., a bunch of nanowires stick together like wet hair upon removal from the liquid. In contrast to wet hair, however, they do not come apart again when dried.

could be expected that the nanowires will not be coated with Cu since they are rather bad conductors, it nevertheless proved to be difficult to produce a homogenous Cu layer on top of the remaining Si substrate. The key to success was rather slow processing with optimized electrolytes and deposition conditions. Basic Cu deposition data were as follows: Electrolyte composition: 300 ml H_2O, 70 ml H_2SO_4, 5 g $CuSO_4$, 0.1 g DTAC (1-dodecyl-trimethylammoniumchloride, 97%), 0.1 g SPS (Bis-3-sodiumsulfopropyl-disulfide), 0.1 g PEG (Polyethylenglycol). The Cu deposition was done at constant 20°C under potentiostatic conditions with a constant applied potential of –0.5 V for times around 10 h.

The long processing times in this case are problematic from cost considerations; in Sec. 4 it will be shown how this problem can be circumvented.

Major Test Results of the Nanowire Anode

The half-cell used for first tests has a Li reference electrode instead of a standard cathode; the separator is a glass fiber fleece. The standard LP-30 (Merck) electrolyte (0.5 ml) consists essentially of dimethylcarbonate and ethylencarbonate (1:1) plus 1 mol/l of $LiPF_6$. The system is mounted under Ar atmosphere into a cylindrical Ti housing and pressed together mechanically.

Test batteries are similar to the half-cell, but use a standard NCM ($LiNi_xCo_yMn_zO_2$) cathode and are laminated into an airtight Al-foils stack. Both half-cell and battery were assembled and tested under standard conditions in the Li ion battery R&D facility of the ISIT/Germany.[23]

In what follows only some basic results are given without much details. Figure 2 shows SEM pictures of Si nanowire anodes after 6 and 66 cycles, respectively. The (beneficial) formation of SEI and the mechanical stability is clearly visible.

These anodes were used in the half-cell described above. Charging and discharging follows standard ISIT procedures, e.g. charging with $C/10$ (with C = nominal capacity and 10 h being the charging time) for the first eight cycles, for the remaining cycles $C/5$ was used as charge/discharge rate.

Figure 2 also shows the Cu layer and the separator material (needed to avoid accidental short circuits between anode and cathode). The nanowire array bends, as could be expected under the circumstances, but no breakage appears to take place during battery operation. Figure 2b, in particular, shows the presence of the necessary SEI (the wavy-looking structure) that eventually will embed and thus stabilize all nanowires.

A satisfying performance was found with most but not all samples. Figure 3 shows the overall performance of a good anode used in an otherwise standard battery design for 66 cycles. The full capacity of Si was realized, the irreversible Li losses are around 14% in the first cycle and thus acceptable, and no detectable loss of capacity was observed.

Not all anodes showed top performance, however. The reason for this was found to be occasional Li leakage into the substrate because the Cu layer was not always absolutely impermeable to Li. In particular, the edges of the sample may "leak", and pinholes in the Cu layer on occasion also provided for local Li leakage to the Si substrate. Li incorporation into the Si substrate generally

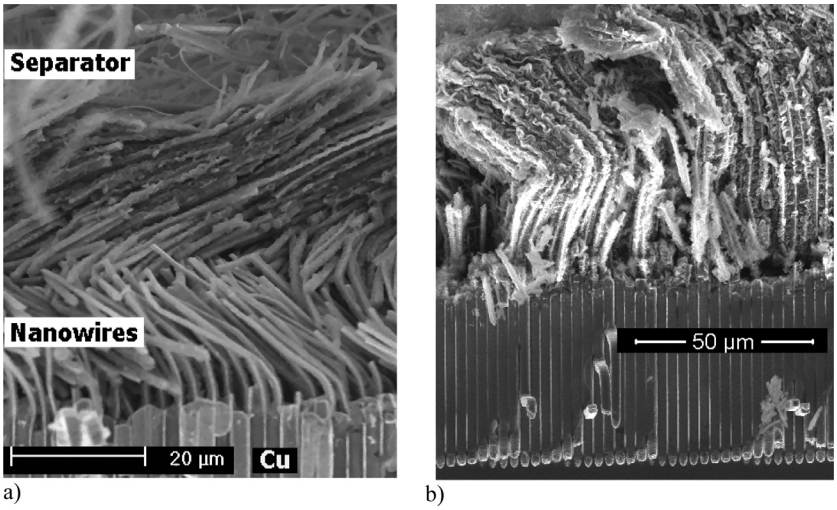


Figure 2. SEM cross-section of Si nanowire anode after 6 cycles (a) and 66 cycles (b) in a half-cell. Note that nanowire breakage occurred during specimen preparation by cleaving and not during operation.

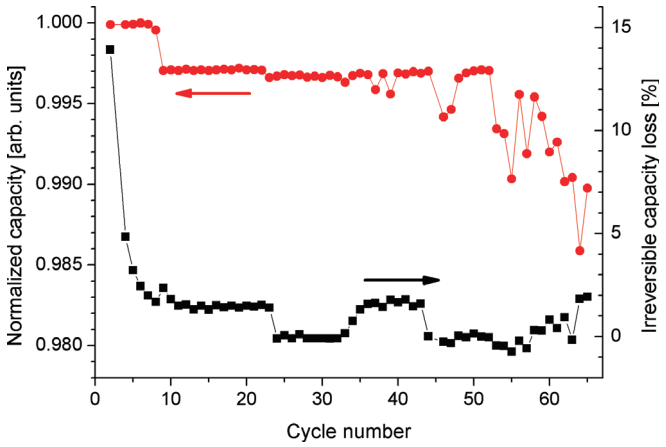


Figure 3. (Color online) Normalized charge capacity (normalized to its maximum capacity, around 4200 mAh/gr) of the Si nanowire anode, and its irreversible capacity loss. Appreciable irreversible losses of up to 13.9% are present mainly during the first 8 cycles, and then the loss is close to zero. The observed negative values of loss in some cycles are due to small leakage currents.

compromises the anode quality during cycling and thus must be prevented. In the following section it will be shown how this effect can be completely eliminated.

Process Improvements

While the process chain described so far demonstrated the general validity of the approach, the process needed to be improved to allow cost efficient mass production of high quality anodes. The authors of this report have accomplished the improvement of the structure of the anodes in several ways, what could be translated into a better performance of the anodes and a reduction of costs. The optimization steps are addressed in the following lines:

1. Optimizing macropore etching.
2. Optimizing the nanowire geometry and the Si efficiency *SE*.
3. Minimizing the processing time for the chemical over-etch and enlarging the process window.
4. Avoiding stiction of the nanowires.
5. Minimizing the processing time for Cu galvanics.
6. Avoiding Li ion leakage to substrate silicon.
7. Optimizing the use of expensive Si wafers.

Progress to point 1 requires "fast" pore etching in large Si wafers (200 mm) under tight process control. All these points have been dealt with in prior work of our group and the reader is referred to 12, 24 and 25).

Substantial progress to the points 2–7 is achieved by etching macropores with diameters that are not constant but vary with depth in a specially tailored way. Again, the necessary hard- and software for etching macropores with variable diameters into 200 mm Si substrates has been developed before in our group,[12,25] and the process is already as fast and cost-efficient as can be.

Point 2 and to some extent point 3 is met by using a KOH (or TMAH) based anisotropic etch under condition where the {110} planes are stop planes for etching ($C_{KOH} = 0.45$ wt %, $T = 50°C$, etching time = 90 min). This principally allows for an optimal *SE* value of up to 0.25. In comparison, pores in a square array with circular cross-sections and isotropic over-etching lead at best to *SE*(square) = 0.21 (see Fig. 4a); an hexagonal close-packed array would have *SE*(hex) = 0.1. Maximum Si usage is thus achieved with the new technique.

The anisotropic etching already reduces the processing time for the chemical over-etch (point 3) substantially. Tapering the pores globally as shown in Fig. 5 provides for further progress. The effect of the global taper is that less Si needs to be dissolved deep in the pores, allowing for a gradient in the dissolution rate as a function of depth. This balances to some extent the slower dissolution rates deep down in the pores because of diffusion limitation. The total effect of the measures taken with respect to points 2 and 3 is an optimal *SE* factor, a reduction of the processing time from ~15 h for the isotropic etch to 1.5 h for the anisotropic etch with global taper. A far larger process window is realized, too, since the anisotropic etch does not have autocatalytic components like the isotropic etch that make the process non-linear and hard to control.

Point 4, the avoidance of stiction, is addressed by introducing pore diameter constrictions, as shown in Fig. 5. Two or more constrictions are introduced at suitable depths of the pores. This requires some complex control of the etching parameters since any constriction will change the subsequent etching behavior during continued pore growth. The effect of the constrictions is clear. Since at the places of the constrictions more Si needs to be dissolved before pore walls touch, limiting the dissolution time will assure that this does not happen at the depth of the constrictions. The result is that a stabilizing Si layer is present between the nanowires that prevents them from touching by stiction. Figure 6 provides a picture of this. One stabilizing layer might not be sufficient to avoid stiction as shown in Fig. 6b, but two or more layers are sufficient, cf. Fig. 7.

The decisive advantage of stabilizing the nanowires against stiction is that the surface is still well defined. This allows addressing points 5–7 in one fell swoop. Copper can now be deposited on the top of the nanowire structure and the resulting copper-nanowire "nanofur" may now be removed from the substrate. The latter step is facilitated by the end tapers shown in Fig. 5a, which ensure that the nanowires are very thin at the meeting point with the substrate as seen in Fig. 6a, showing a removed layer upside down. Figure 8a shows Cu on top of the nanowires and Fig. 8b a peeled off "nanofur". The "nanofur" is a finished anode; all that remains to be done is attaching it to a current collector.

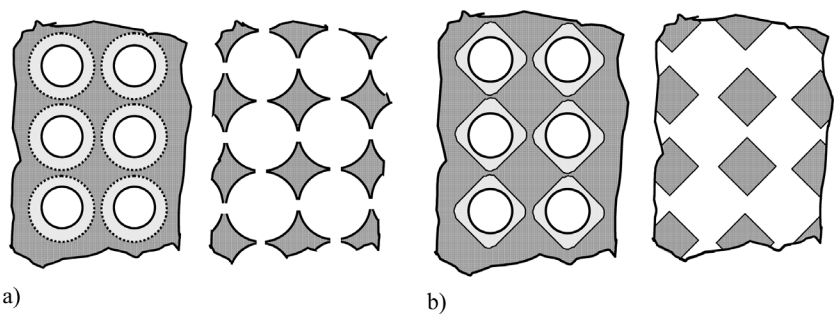


Figure 4. Macropores in a square array (white circles) and the resulting nanowire structure after (a) isotropic over-etching (shaded circles) and (b) anisotropic over-etching.

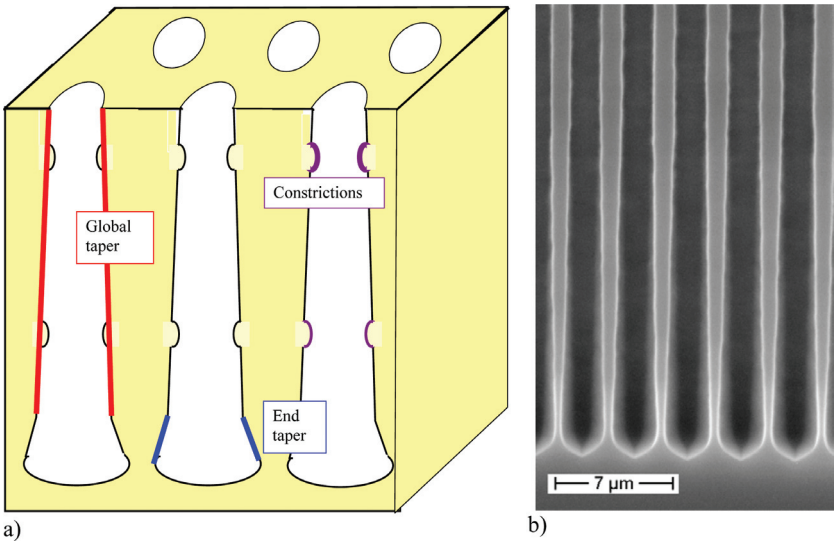


Figure 5. (Color online) (a) Tailoring the macropore diameter. The global taper re-duces over-etching time, and the constrictions provide the stabilizing planes preventing stiction. (b) Pores with end taper.

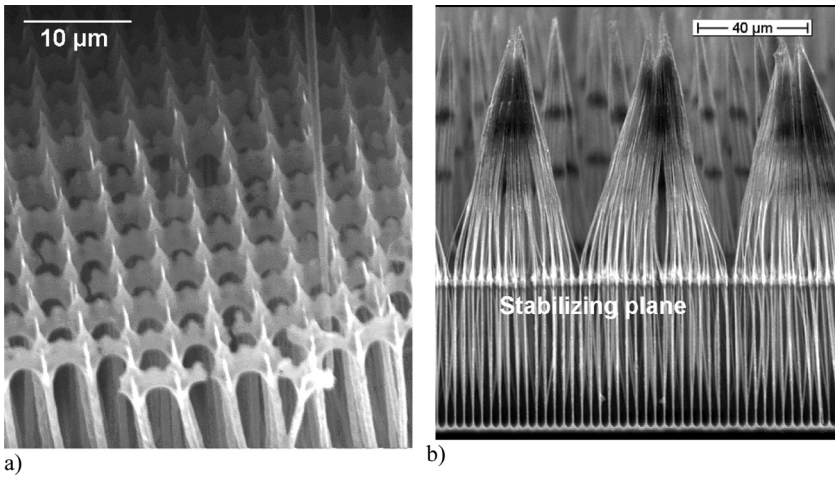


Figure 6. (a) Looking at the bottom of a detached nanowire array with a clearly visible stabilizing layer. (b) Effect of one stabilizing plane on stiction effects.

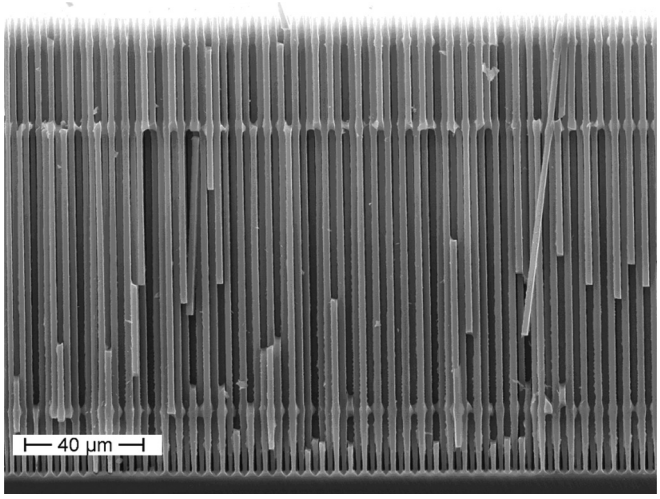
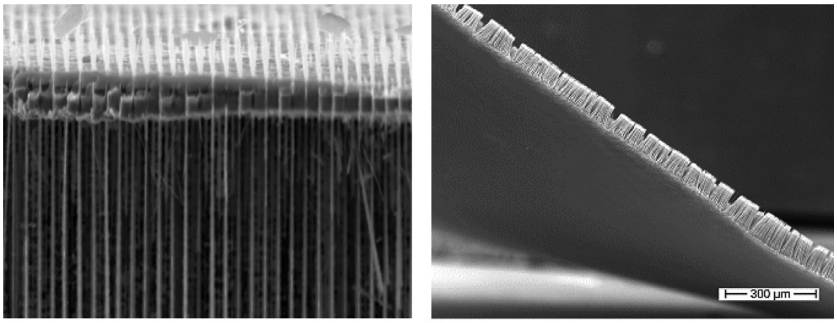


Figure 7. Fully optimized nanowire structure with SE ≈ 0.5, two stabilizing layers preventing stiction and decreased diameters close to the substrate.

The Si substrate after detaching the "nanofur" can be reused; point 7 thus has been successfully addressed, too. Leakage problems (point 6) cannot occur anymore because there is no bulk Si left.

Cu deposition on top of the nanowire array is in principle far easier and faster than at the bottom but provides some challenges on its own. While Cu deposition by some sputter technique could easily produce a coherent Cu layer with a thickness of several μm, the process is neither fast nor cheap. In addition, Cu adherence to Si is a (known) problem that may necessitate some intermediate layers such as TiN. The approach we pursue at present with some success (see Fig. 6b) is therefore electroless plating a seed layer followed by standard Cu galvanics; a fast and cheap process sequence. Simply immersing the nanowire array while still connected to the Si substrate into suitable Cu bath will deposit Cu electroless only on the nanowire tips because of diffusion limitation into the depth of the nanowires. To facilitate Cu deposition even more, a stabilizing layer can be introduced close to the top of the nanowires, providing a closed surface and a very efficient diffusion barrier. As soon as the top of the nanowires is covered with Cu, the path for Cu deposition deeper down is closed. This was one of the major problems



a) b)

Figure 8. (a) Cu layer on top of the nanowire array deposited galvanically after electroless formation of a Cu seed layer. (b) A partially peeled off "nanofur" leaving a reusable substrate behind.

encountered when depositing Cu deep down in pores of nanowire arrays but works to our advantage now.

Conclusion and Outlook

The process chain introduced in this paper establishes a technology base that lends itself to cheap mass production of Si nanowire anodes for Li ion batteries. The complexity of processing a 200 mm wafer is roughly comparable to that of a solar cell and can thus be projected to be around a few Euro after mass production has been established. The capacity of a 200 mm "nanofur" anode with an active nanowire length of 150 μm, an *SE* factor of 0.25, and a Si weight of 2.3 g will be around 10 Ah. Assuming conservatively an average voltage of 2.5 V, we have an energy density of 25 Wh, which seems to be sufficiently large to warrant further work.

It is clear that upscaling the process to a 200 mm technology requires substantial work, time and money. Nevertheless, we are confident that large-area Si nanowire anodes can be made and tested within the next year.

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