Journal of The Electrochemical Society, **161** (12) D657-D662 (2014)
0013-4651/2014/161(12)/D657/6/$31.00 © The Electrochemical Society

Enhancement of Cu Filling into p-Type Macro-Porous Silicon by Pore Wall Thinning, Oxide Deposition and Back Side Illumination

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Electrochemical deposition of Cu on structured silicon including groves and pores is critical for several applications such as microelectronics, sensors, and energy applications. In the case of Cu filling of porous Si, the silicon skeleton can be either etched to produce free nano- or micro-structured Cu or can be left to form a nano- or micro-composite of Si/Cu. Deposition of metals into n-type porous Si is a relatively straight-forward process, due to the availability of electrons at the conduction band to reduce Cu cations. Cu deposition into p-type porous Si requires illumination, unfortunately, it enhances the growth on pore walls and results in either non-conformal growth or plug-in which lead to voids. In this work, it is shown that illuminating the back side of the wafer combined with insulating the pore walls and pore top leads to conformal growth of Cu from the pore-tip to the pore-top. Two approaches have been tested: wall thinning by chemical etching and SiO_2 coating on the pore top. Massive wires have been obtained by completely and conformally filling porous Si without leaving gaps in the case of SiO_2-coated samples. The conformal filling of p-type Si was obtained without using additives and without seed layer.

Manuscript submitted June 9, 2014; revised manuscript received July 31, 2014. Published August 20, 2014.

Metallic micro- and nano-structures such as ordered rods and tubes can be fabricated via filling a template with a single metal or an alloy. The resulting structures can be used in a wide range of applications including energy and sensing devices. For example, for energy applications, using arrays of Cu rods as current collectors for electrochemically synthesized SnCo alloy shell anodes enhanced their performance in lithium-ion batteries.[1] A common approach to fabricate arrays of nano- or micro-wires, rods or tubes of any material, is to deposit the material into a porous template, and then dissolve the template.[2] The template can be an ion-track-etched membrane,[3] anodic aluminum oxide[4,5] or other porous material such as porous Si.[6,7] Using porous Si enables on-chip fabrication of either metal-Si composites,[8] or metallic wire or rod structures.[9]

Because porous Si fabrication is a well-established technology and Si can be easily etched to produce free standing metallic structures, filling porous Si with metals and other materials has attracted the attention of many research groups. Porous Si as regular nanostructured material has been used for electrochemical preparation of binary and ternary nanostructured compound systems.[10] In some cases it has been observed that the electroless deposition oxidizes porous Si simultaneously,[11] therefore electrochemical deposition is preferred to fill porous Si. During cathodic metal deposition the oxidation of porous Si is prevented and the metal content inside the pores is higher compared to electroless deposition approaches.[11]

Illumination allows metal deposition of Ni in p-type porous Si, while no deposition is obtained in darkness, since only electron injection from the conduction band (after excitations of carriers from the valance band to the conduction band) contributes to Ni reduction, due to its high redox potential.[11] Laser photo-excitation of porous p-type Si has been used to local electrodeposit Ni into it.[12] In contrast, n-type meso- and macro- porous Si has been filled with Ni and Cu without the need of illumination.[13–15] No illumination is needed for deposition on n-type Si since electrons are the majority carriers. Illumination results in an increase of the electron population in p-type Si, enhancing the deposition (or allowing it, in the case of Ni). The difference in the redox potential between Cu and Ni is just notorious as effect when electrodepositing on p-type Si.[16–22] Illumination has been used to fabricate Cu micro- and nano-wires/tubes; it allows controlling the growth to be either from bottom to top of pores, or on the pore walls of p-type porous Si.[19,23] Cu grew at the pore bottom in dark, while Ni did not grow; but as the light switched on, growth of Ni at pore walls was obtained.[19] Without illumination, the electrochemical deposition of Cu into p-type macroporous Si requires high potentials for injecting holes into the valance band of Si to reduce the Cu^{2+} ions at its surface. Moreover, even if it is possible to deposit Cu in darkness, the application of high potentials increases the probability of Cu nucleation on the pore walls especially near to the pore top, which leads to necking and hence plug-in. Electrodeposition of Cu into macroporous Si is not a common process, and just a few reports can be found in the literature,[11,18,19] showing that the challenge of bottom-to-top filling of pores still requires investigation and development. Refs. 11 and 18 show that noble metals such as Cu are deposited into p-type macropores in dark by hole injection from the valence band, and under illumination by electron injection from the conduction band. No conformal filling with high aspect ratio is shown in,[11] while in Ref. 18 conformal filling of Cu in dark is demonstrated, but without comment on aspect ratio. High aspect ratio deposition of Cu into p-type pores has been achieved in darkness condition in Ref. 19. In the same reference it was described that Cu filling takes place under back-side illumination due to electron injection from conduction band, but it leads to growth both at pore bottom and on pore wall as well.

In this work pore filling of p-type macroporous Si under illumination conditions is studied. Additionally, two approaches have been tested for diminishing Cu growth on pore walls or at the top of the pores. The first method consists in thinning the pore walls, so they could present overlapping space-charge-regions that have an isolating effect; the second method is the deposition of an isolating layer (SiO_2) at the top of the pore walls avoiding deposition at these areas reducing necking effects. We achieved massive wires by completely and conformally filling porous Si (30 μm deep pores with an aspect ratio of 12) without leaving gaps in the case of SiO_2-coated wall under illumination.

Experimental

(100) p-type Si wafers with resistivity 15–25 Ωcm were used as starting material for the production of the porous Si templates. After pre-structuring of the Si wafers by standard photolithography, and KOH etching of inverted pyramids (see Ref. 24 for further details), macro-porous Si was etched in dark. The structure defined by lithography was a quadratic array of circles with 3 μm pitch. The etching electrolyte consisted of 210 mL Dimethylformamide (DMF), 60 mL de-ionized (DI) water, 30 mL HF and 2.5 g Polyethylene glycol (PEG) 3400. The temperature was kept constant at 17°C for the etching process. Wafer pieces were etched on a circular area of 0.78 cm^2 in a commercially available electrochemical processing station from ET&TE GmbH.[25] The current profile was adjusted to produce 30 μm deep pores with a pore diameter of 2.5 μm (aspect ratio of 12).

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For some samples the pore wall was thinned using anisotropic chemical etching of silicon in two steps: i) passivation by immersing the porous sample in a solution of 1 L DI water and 50 g PEG for 30 min at 50°C. ii) Etching the porous Si walls in a solution consisting of 100 mL DI water, 2 g PEG and 0.45 g KOH at 50°C for a duration of 30 min.

Samples covered with SiO_2 were obtained by depositing the oxide films by plasma enhanced chemical vapor deposition (PECVD) using a SENTECH 550 PECVD system at 300°C with SiH_4 and N_2O as precursor gases. The thickness of the layers, measured by ellipsometry, was 100 nm.

For the electrochemical deposition of Cu into porous Si, the same electrochemical cell employed for etching was used. Just the polarity was reversed since Cu deposition takes place in the cathodic biasing region, in contrast to the electrochemical etching of p-type Si, which takes place under anodic bias. All values of current presented in this work are for an effective deposition area of 0.78 cm^2; values of current are used through the paper instead of current densities. The electrolyte for Cu deposition consisted of 220 mL DI water, 6.25 g $CuSO_4$ and 24 mL H_2SO_4. The temperature was kept at 35°C during the electrochemical plating. The filling experiments were done without using additives and without seed layer, to reduce the number of variables and better discriminate between effects. The deposition was done in darkness and under illumination conditions. The process in dark was performed on samples with Al back side metallization, while for back side illumination Al was chemically removed with an aqueous solution of 10 wt% HF from the area corresponding to the porous section on the front side. For back side illumination, an array of infra-red light emitting diodes (IR-LEDs) of 830 nm light was used; infra-red light is a common light for etching, due to its penetration length in Si.[15,26] The samples were investigated by optical microscopy and with a Philips XL series scanning electron microscope (SEM).

Results and Discussion

Cu deposition under darkness conditions.— Figure 1 shows the *I-V* characteristics of the Si - Cu electrolyte system. A voltage sweep from 50 V to –20 V was performed. Four voltage regions can be identified in the plot. Obviously, applying a cathodic potential to the Si substrate allows the deposition of Cu, which is dissolved when the polarity is reversed. High voltages are necessary for depositing Cu. After some Cu grow on the Si surface at high voltages (region 1), it is easier to get dielectric breakdown, which produces a higher current (region 2), accelerating the Cu deposition. When the potential is further decreased, the current decreases exponentially until a base leakage current is obtained (region 3), where deposition due to minority carriers occurs. Afterwards, when the polarity is reversed, (region 4, anodic range), there is a current peak at which probably most of the previously deposited Cu on Si dissolves, after which the (negative) current decreases again to the values derived from Si/electrolyte depletion.

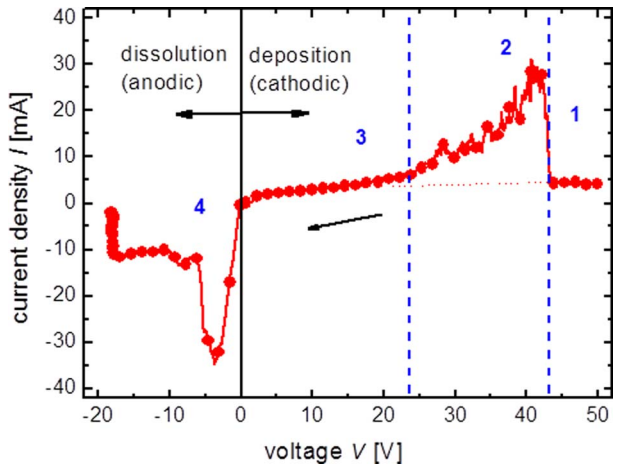

Figure 1. I-V curve of the Si-Cu electrolyte system. Cathodic potential allows the deposition of Cu, which is dissolved when the polarity is reversed. High voltages are necessary for depositing Cu.

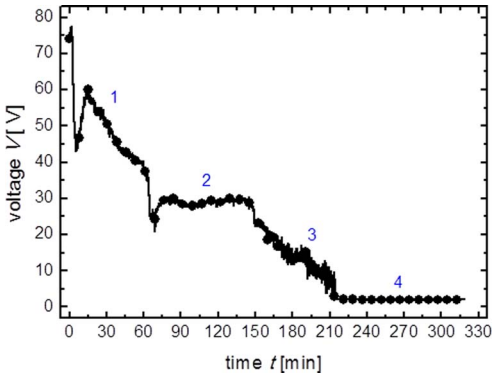

Figure 2. Voltage of the deposition cell during the Cu filling under dark conditions at 4 mA. After 60 min the pore-tip is completely filled (phase 1) and the growth proceeds toward the pore-top (phases 2 and 3). After 210 min Cu grows mainly on the surface of the porous sample (phase 4). Voltage decrease in region 2 could be due to new nucleation sites on pore-walls which increases the reaction area again similar to phase 1.

To deposit at the same rate during the deposition time, independently of the potential, galvanostatic conditions were tested. Figure 2 illustrates the voltage response when depositing at 4 mA (5 mA/cm^2) constant current. SEM images of the obtained deposition after 60 min and 320 min are shown in Figure 3. In the beginning of the

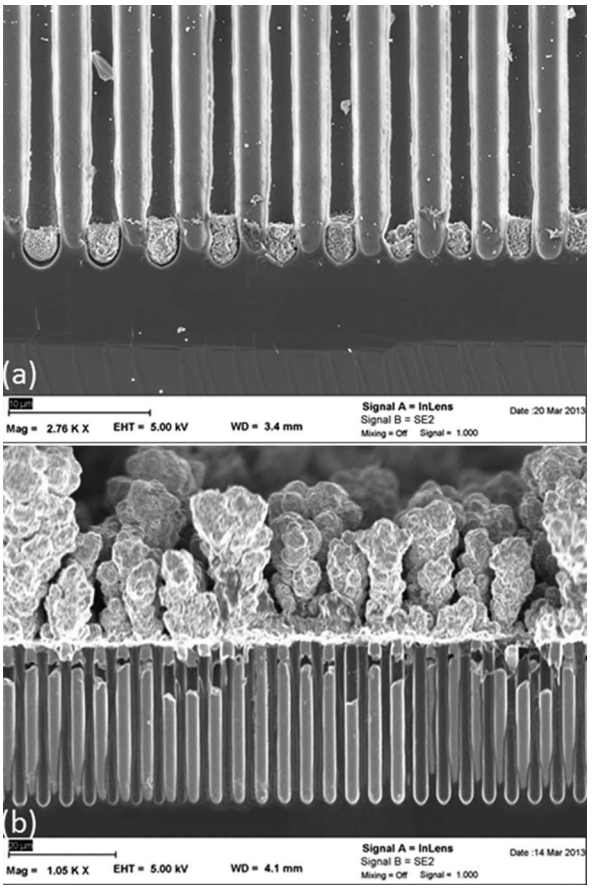

Figure 3. Cross-sectional scanning electron micrograph of electrodeposited copper into porous Si in dark at 4 mA (a) 60 min and (b) 320 min.

cathodic deposition, a very high voltage above 50 V is needed to flow a current of 4 mA (Figure 2, phase 1). In this phase, nucleation at small areas at the pore-tip takes place and the voltage starts to decrease with increasing the metallization area at the pore tip. The monotonic decrease of the voltage with time is due to the monotonic increase of the area covered by Cu on the Si pore-tip. Once the pore-tip is covered by Cu and the cross-sectional area stop to increase (see Figure 3a), the current shows a plateau (phase 2). The voltage decrease in phase 3 is probably due to growth on pore walls after a while (see supporting material Figures S1g-i), which means that the growth area increases and hence the current drops. This explanation is supported by the observed plug-in in Figure 3b, which indicates a growth on pore walls, but in later phases. After the pores are completely filled, Cu growth on a large flat area of Cu needs very small voltages (phase 4). The observed columnar growth in Figure 3b (and in Figure S1 of the supporting information) indicates that the growth rate was too high.

The huge potential needed to flow cathodic current across the p-type Si/Cu electrolyte system is due to the lack of electrons required to reduce the Cu^{2+} according to the reversible reaction

$$Cu^{2+} + 2e^- \Leftrightarrow Cu\,(s). \qquad [1]$$

As there are no conduction electrons in darkness in p-type Si, just the electrons allocated in the valence band may contribute to the reduction process of the Cu^{2+} ions. Injecting valence band electrons into the electrolyte can be represented as hole injection into Si. Hence, the reaction in 1 can be re-written as

$$Cu^{2+} \Leftrightarrow Cu\,(s) + 2h^+. \qquad [2]$$

Figure 4 schematically represents the p-type porous Si in contact with Cu electrolyte under cathodic bias of Si, indicating the possible reaction mechanisms contributing to Cu deposition. The different reaction mechanisms will have the symbol (***R***) through the manuscript. The symbol will have a subscript **T** (which stands for tip), when the reaction is supposed to takes place at the pore tip or **W** (which stands for wall), when the reaction is supposed to take place at the pore wall. The superscript **V** (which stands for valence), when the reaction takes place by hole injection from the valence band, and **C** (which stands for conduction) when electron injection from conduction band

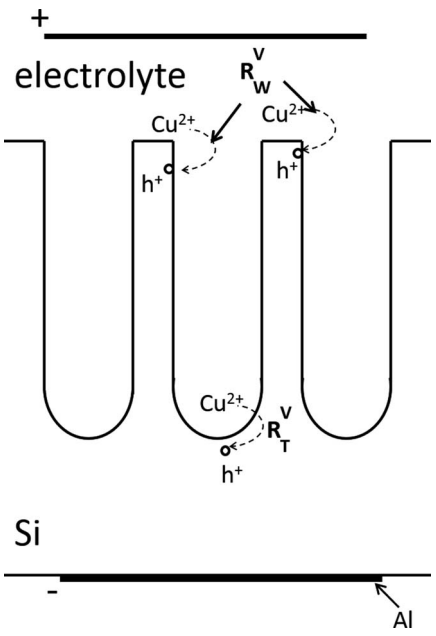

Figure 4. Schematic of p-type porous Si electroplating in Cu^{2+} containing electrolyte in darkness. Reduction via hole injection into the valance band of Si either at pore tip (R_T^V) or wall (R_W^V) which is responsible for deposition in dark.

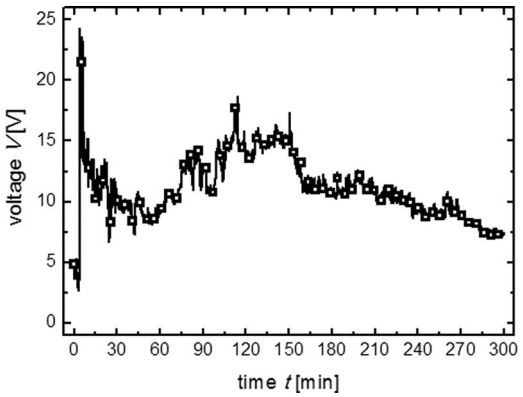

Figure 5. Voltage of the deposition cell during the Cu filling under illumination conditions at 4 mA.

is responsible for the reaction. The reaction described in (2) can take place either at the pore-tip (R_T^V) or at the pore-wall ($\mathbf{R}_W^V$) through the valence band. In darkness, the only way to reduce the Cu^{2+} at the silicon/electrolyte interface is by injecting holes into the valence band of silicon, which is equivalent to extracting the valence electrons. This process requires very high potentials and can take place either at pore-tip ($\mathbf{R}_T^V$) or -wall ($\mathbf{R}_W^V$). Since deposition rate is slow, and the needed potentials are very high in darkness conditions, tests illuminating the back side of Si have been performed, in order to generate additional electrons, as discussed in the next section. If the back side of the silicon substrate is illuminated by long wavelength (IR), as will be shown in the next section, electron-hole generation takes place. The generated electrons diffuse toward the pore-tips and even can exceed it to the pore-walls as high quality single crystalline silicon possess high minority carriers diffusion length which is in the order of the wafer thickness. Therefore, back side illumination will be used in the rest of this work to reduce the deposition voltage by utilizing conduction band electrons for the Cu^{2+} reduction. Then, section 3.3 will investigate two methods to eliminate the Cu^{2+} ions reduction taking place on the pore walls to achieve the tip-to-top Cu growth.

Cu deposition under illumination.— Figure 5 shows the voltage response when depositing at a constant current of 4 mA, applying illumination. Comparing with the voltage obtained during deposition in darkness at the same current (Figure 2), the voltage was reduced from 50 V to about 15 V when applying illumination. In addition to the potential reduction, illumination plays an important role in depositing Cu into the pores instead of depositing on the pore top. Figure 6 compares the current/voltage characteristics for Cu deposition in darkness

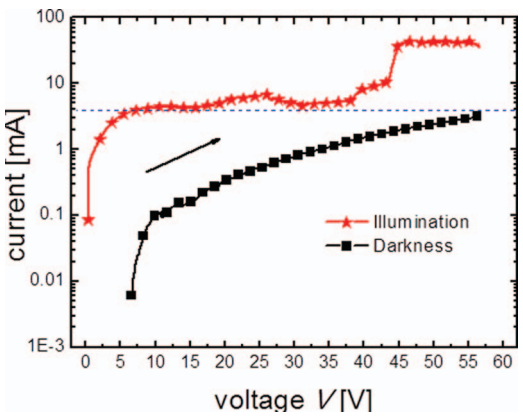

Figure 6. Dark and back-side illuminated current/voltage curves of cathodic plating of p-type porous Si in Cu^{2+} electrolyte. The dashed line indicates the current of 4 mA, used for the experiments of Figure 2 and Figure 5.

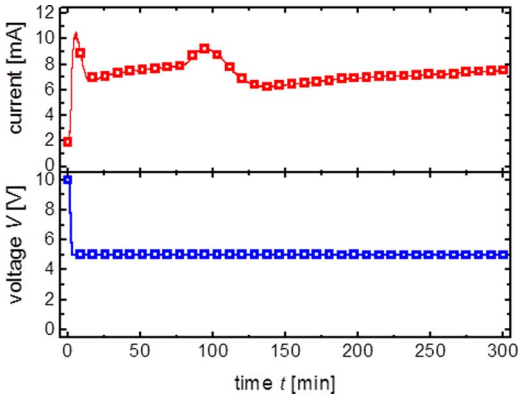

Figure 7. Current profiles during potentiostatic Cu deposition under back side illumination.

and Si-back-side illuminated conditions. From the image it is clear that for getting a current of 4 mA (as for Figure 2 and Figure 5) just 5 V are necessary when applying illumination, while over 55 V are needed without illumination. The sudden increase in the current for the illuminated case in the range between 45 and 55 V is not fully understood, however it is probably related to growth on the sample surface, after the pores are filled or after the pores are closed. This point is out of the focus of this paper and may be investigated in a separate study. The conclusion of this experiment is that illuminating the back-side of p-type silicon during Cu deposition enables decreasing the voltage by a factor of 10 in the galvanostatic deposition, or increasing the current by the same factor in the potentiostatic case. This observation is confirmed by modulating the back side illumination as shown in the supporting material in Figure S2, while the voltage profile was recorded as a function of time during galvanostatic experiment. About 20 V reduction was observed in the voltage response when Si was illuminated.

An optimized voltage profile to fill the pores from tip-to-top was obtained after a series of tests. The profile consists of constant high voltage of 10 V for short time (5 min) for initiating the nucleation of a Cu layer, and then keeping the voltage constant at 5 V for about 300 min for further deposition. Figure 7 depicts the current and voltage measurements when depositing with the proposed voltage deposition profile. In the nucleation phase, the voltage of 10 V forces the increase of the current from 2 up to 10 mA. After decreasing the driving potential to 5 V, a drop of the current takes place and then it stabilizes in a moderate range. The enhancement of the current flow can be ascribed to the generated electrons (excitation of electrons to the conduction band) due to back-side illumination. The generated electrons diffuse toward the pore-tips, and in a lower degree even to the pore-walls; high quality single crystalline silicon possesses diffusion lengths in the order of the wafer thickness. Therefore, the conduction band electrons contribute to the Cu^{2+} reduction at the interface at smaller voltages through the reactions at pore-tip ($\mathbf{R}_\mathbf{T}^\mathbf{C}$) or at the pore-wall ($\mathbf{R}_\mathbf{W}^\mathbf{C}$) as shown schematically in Figure 8.

Using the optimized voltage profile of Figure 7 for the deposition under illumination, in some cases the deposition started on the top of the pores instead than on the pore tips. This can be attributed to leakage currents. The leakage current contributes to the reaction ($\mathbf{R}_\mathbf{W}^\mathbf{C}$), which leads to a growth on pore walls and the top area between pores. To enhance tip-to-top Cu wire growth, it is necessary to shut down the reactions at the pore walls ($\mathbf{R}_\mathbf{W}^\mathbf{V}$) and ($\mathbf{R}_\mathbf{W}^\mathbf{C}$). The following section investigates two approaches to reduce those reactions.

Reducing leakage currents during Cu filling.— In some cases, under darkness or illumination conditions there was deposition on the walls and the pore tips at the same time. This is a problem for uniform pore filling, since some pores could be closed earlier and some branching may start to occur on the surface of the samples, as observed in Figure 3b and supporting images S1g and S1i. In this

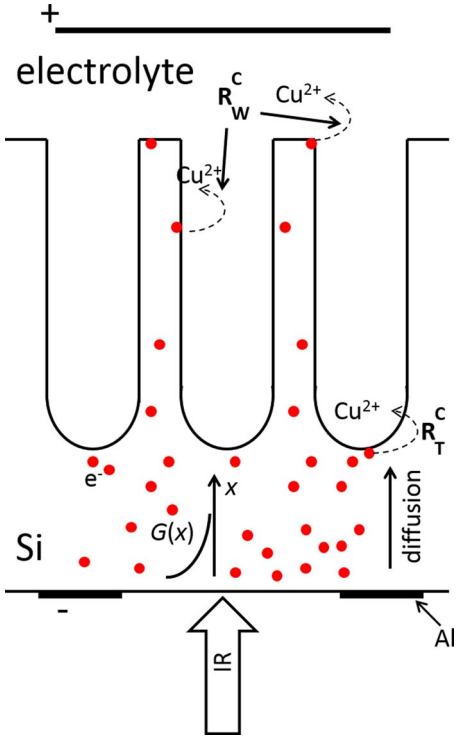

Figure 8. Schematic of the p-type porous Si electroplating in Cu^{2+} containing electrolyte under back side illumination. Reduction of Cu^{2+} via electron injected from the conduction band into the electrolyte at the pore tip ($\mathbf{R}_\mathbf{T}^\mathbf{C}$) or wall ($\mathbf{R}_\mathbf{W}^\mathbf{C}$) occurs.

work two alternative approaches to decrease the leakage currents at the pore walls and at the top section between pores are investigated. They enable a tip-to-top Cu growth into p-type porous Si. The first approach is to deposit an insulating layer such as SiO_2 on the top spaces between pores. The second approach is to make the pore walls thin enough to be depleted during the cathodic biasing. The later approach is challenging because the pore walls should be very thin, what makes them mechanically unstable.

Coating porous Si with SiO_2 made illumination necessary for copper deposition. In darkness the observed current is only the leakage current that probably does not contribute to reduction reactions of Cu cations on silicon (see supporting material Figures S3 to S4). An optimized voltage profile was developed based on series of experiments and the understanding of the Cu/Si junction behavior (Figures S6 and S7). Figure 9 presents a comparison of the current response during Cu deposition using the developed voltage profile shown in Figure 7 for three different cases of porous Si, under the same back illumination level: The first case is bare porous Si, the second is porous Si coated with 100 nm SiO_2 at the pore top, and the third one is wall-thinned porous Si.

For the wall-thinned sample the current was even lightly higher than for the untreated sample, thus the reaction ($\mathbf{R}_\mathbf{W}^\mathbf{C}$) at the pore walls was not eliminated. The wall-thinning was not able to make pore walls insulating because pore walls are probably still wider than required to cause carrier confinement. The pore wall was decreased from 2.4 μm to 0.8 μm after 30 min etching as described in the experimental part. Etching longer than 30 min resulted in pore collapse; therefore thinner pores were not able to be tested. On the other hand, the current increase may be caused by two reasons: The first reason is the increase of the pore surface area due to decreasing the pore walls. The second reason is that there is more electrolyte available, and the diffusion of electrolyte is less limited due to the wider pores.

On the other hand, we succeeded to make the top of the pores insulating by depositing 100 nm SiO_2 on top of porous Si. The drop

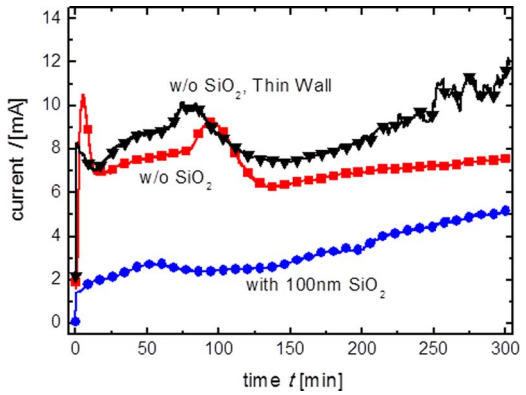

Figure 9. Comparison of current profiles during potentiostatic Cu deposition under back side illumination, when depositing SiO_2 on upper part of the walls and when thinning the walls. The result when no treatment is done is also shown.

of current from 10 to 2 mA at the beginning of the deposition process due to coating porous Si by SiO_2 indicates that the pore walls were still conducting and deposition was taking place on walls without insulation. In this case, the monotonic current increase observed in Figure 9 in the case of 100 nm SiO_2 is attributed to the resistance decrease inside the pores due to Cu growth inside them.

Figure 10 schematically explains our two approaches to make pore walls insulating to shut-down deposition reactions on pore walls during the electroplating of p-type porous Si under back side illumination. Reduction of Cu^{2+} via electrons injected from the conduction band into the electrolyte at the pore wall ($\mathbf{R_W^C}$) can be inhibited either by thinning the pore walls (Figure 10a) to reduce conduction of electrons by carrier confinement, or by depositing an insulating layer such as SiO_2, on the top part of the pores (Figure 10b). Nevertheless, in the present work just the second approach worked efficiently. In this case, after the nucleation phase, the tip-to-top filling of the pores led to a monotonic increase of the current as the distance from the Cu/electrolyte interface propagates toward the pore-top causing a decrease of the total electric resistance. SiO_2 is not the best isolating material, but it is easy to obtain and is fully compatible with the Si technology. In spite of the not-perfect masking properties of SiO_2 for Cu plating, we achieved a conformal filling of pores. We believe the reason for that is that SiO_2 further reduces the conductivity of pore-walls to a certain value which allows for Cu growth from the bottom of the pores to their top. The micrograph in Figure 11 shows an example of sample where Cu was grown into SiO_2–coated p-type porous Si with the optimized voltage profile, under back-side illumination. The Cu forms massive wires by filling completely and conformally porous Si without leaving gaps.

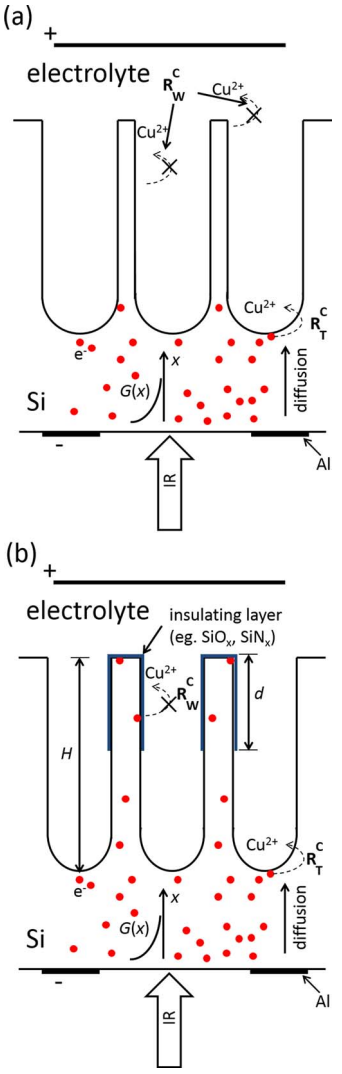

Figure 10. Schematic shows the electroplating of p-type porous Si in Cu^{2+} containing electrolyte under back side illumination. Reduction via electron injected from the conduction band into the electrolyte at the pore tip (R_T^C) or wall (R_W^C), which takes place under illumination. Reduction via electron injected from the conduction band into the electrolyte at the pore wall (R_W^C) can be inhibited either by (a) thinning the pore walls to reduce conduction of electrons by carrier confinement or (b) by depositing an insulating layer, such as SiO_2, on the top part of the walls.

Conclusions

Two methods to enhance the Cu filling of macroporous p-type Si from pore bottom to top during electrochemical deposition using back-side illumination were tested. Enhancing the Cu growth was on the base of isolating the pore walls to shut-down the reduction reactions of Cu cations at the walls. Wall isolation was performed by wall thinning and by coating their top section with SiO_2. Nevertheless, the wall thinning did not work for reducing the Cu deposition on the pore walls in this work, probably because they were still too thick to cause carrier confinement. The walls were still conducting, and the current during deposition was in the same range as for bare macroporous Si. In contrast, the best pore filling was achieved in the case of the SiO_2 coated sample. In this case, massive Cu wires were obtained by completely and conformally filling porous Si without leaving gaps. In spite of the pore masking properties of SiO_2 for Cu plating, we achieved a conformal filling of pores. We believe the reason is that SiO_2 further reduces the conductivity of pore-walls to a certain value

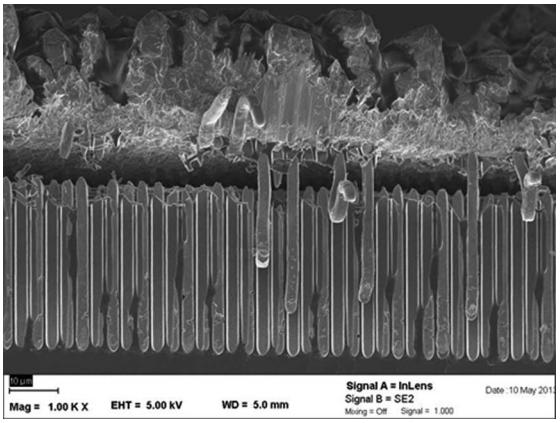

Figure 11. SEM micrograph of Cu filled SiO_2-coated porous Si. The quality of Cu is good and the upper Cu forms a massive film.

which allows for Cu growth from the bottom of the pore to its top. We did not use barrier materials, or additives in the plating solution. For differentiating effects, it was better not to use additives. However, for further improving the deposition, we may try with additives in future investigations.

Acknowledgments

The authors thank Iris Hölken, Emmanuel Ossei-Wusu and Mark-Daniel Gerngroß for their help with some proceedings and for fruitful discussions.

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