Electrochemical Fabrication and Characterization of Silicon Microwire Anodes for Li Ion Batteries

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With a technique allowing for large-scale production, which is based on electrochemical etching, silicon microwire anodes for Li ion batteries anodes are produced. The wires exhibit high areal capacity due to their diameters in the micron-range, and high cycling stability due to the formation of a homogeneous solid electrolyte interface around each of them. This study summarizes the importance of the (exact) battery work parameters and their dependence on the wire dimensions. Furthermore, it compares two anode concepts in which the wires can be incorporated. FFT-impedance analysis shows the characteristic resistance changes under specific conditions, which relate directly to the processes in the wires during operation, what helps for their optimization.
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Among different anode materials, nano- or microstructured Si have become increasingly important in recent years. Compared to graphite anodes, Si anodes posess a more than tenfold gravimetric capacity of 4200 mAh/g.[1–3] This capacity can be stable over hundreds of cycles if Si is in the form of nano- or microwires. On the other hand, if it is in bulk state, large cracks could form during cycling due to large volume expansions, leading to open circuits in batteries in a few cycles.

Different techniques like standard vapor-liquid-solid (VLS)[4,5] and metal assisted electroless chemical etching methods (MACE)[6] can be used to structure Si. Nevertheless, in the most of the works with these techniques, wires randomly distributed are presented. A random distribution of sizes and spacings of the wires limits the battery performance because the diffusion of Li into the wires is not homogeneous.

Due to progress in the electrochemical pore formation in n- and p-doped Si by different groups around the world, homogeneous, nano- and micro-structured Si can be produced. With the anodic etching of Si in various electrolytes, different pore structures have been developed.[7–11] In this study electrochemical pore etching and chemical over-etching processes for the production of wire arrays for battery anodes were optimized in order to obtain a silicon wire array with intergrown stabilizing planes. The wire arrays, when used as anodes of batteries, withstand large stresses, and present a stable capacity of 3150 mAh/g for over 100 cycles with an areal capacity of 4.25 mAh/cm^2,[1] a record among Si anode concepts. It is well known that graphite anodes suffer from a continuously growing solid electrolyte interphase (SEI) which forms due to the decomposition of the electrolyte, thus hindering further intercalation of Li in the graphite. Astonishingly for the silicon microwire anodes discussed in this paper, we found that the SEI stops to grow after the first three charge/discharge cycles, which is one reason for the good cycling stability.

This paper deals with the fabrication and electrochemical characterization of the Si microwire anodes, emphasizing the importance of the wire dimensions, which determine the optimum charging/discharging conditions of the anodes. Depending on the size of the wires, the characteristic potentials and impedances are given. For this study, besides the Si microwire array anodes, also paste electrodes have been produced with the same microwires; this allowed a simpler electrochemical characterization of Si microwires of different sizes without the need of optimizing Cu deposition on the wires (a needed step for the array anodes). Cyclic voltammetry and FFT impedance spectroscopy (FFT-IS) have been used for the electrochemical characterization.

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Processing of Si Microwires

The basic fabrication steps are the same for preparing the Si microwires for both, arrays anodes and paste electrodes.

The method for the fabrication of Si microwires consists of a series of electrochemical and chemical etching steps on Si wafers (commonly p-type (100)). All of these steps need a pre-structuring step of peaky tips that work as nucleation points for the electrochemical etching. This can be accomplished by standard photolithography, followed by anisotropic dry and wet (chemical) etching steps to allow the formation of inverted pyramids.[12] The electrochemical etching is based on the anodic etching of silicon and can be applied/designed with various electrolytes. Typically, the electrolytes consist of 5 wt.% HF with an addition of an organic solvent like dimethylformamide (DMF). In some experiments, to facilitate the variation of the diameter of the wires, water was added to the etchant. With the addition of water, SiO_2 is formed electrochemically at the pore walls, and is dissolved chemically by HF. The process of oxide formation and dissolution is continuous over the etching process.[13,14] This etching modus allows obtaining wider pores (thinner walls). Without the addition of water, the oxidation process is limited, and direct dissolution of silicon is performed, preferentially at the pore tips (producing thinner pores).

The pores must be modulated to allow the formation of stabilizing planes at the end of the fabrication process. Pore modulation is obtained by varying the current density over time, and is enhanced through the addition of polyethylenglycole (PEG), which passivates the pore walls and reduces their over-etching (etching is focused at the pore tips).[4,15] By applying a specific current-time profile to the sample, the pores can be modulated according to length and diameter. Figure 1 shows examples of current profiles for obtaining wires with different lengths, with two pore narrowings (obtained by steeply reducing the current). The length can be varied from short pores (36 μm) to longer pores (130 μm) by adapting the etching time and current.[5,6]

To obtain the wires from macroporous Si purely chemical post etching of the pore walls is used. This chemical etching is performed with an etchant with a low concentration of KOH.[1,4] The longer the etching is performed, the thinner the wires. The limit of the wire thickness is around 900 nm, when the stabilizing supports are etched away and the wires start collapsing. The combination of both, the electrochemical and chemical etching steps allows the production of wires with various lengths and thicknesses. The process is also scalable to obtain wire arrays over different areas. The sample area can be varied by modulating the etching current and controlling the temperature.[16] As discussed before, the electrochemical and chemical etching steps are for both anode configurations the same.

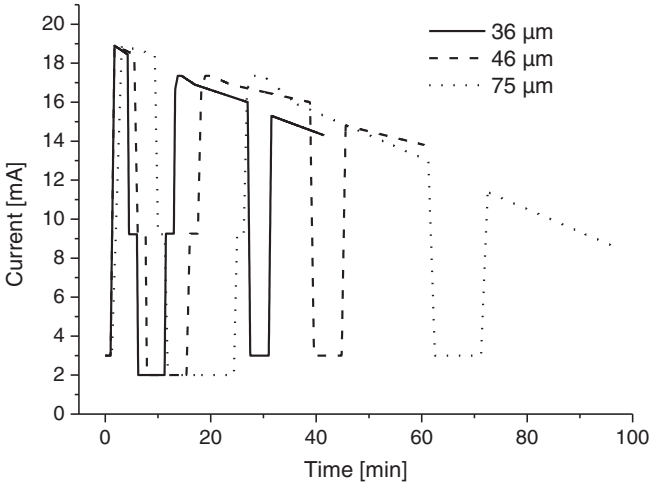

Figure 1. Electrochemical etching profile adapted for various pore lengths, ranging from 36 to 75 µm.

Production of Battery Anodes with the Si Microwires

Paste anodes.— In order to test lithiation/delithiation as a function of wire thickness a simple paste electrode was fabricated. The paste electrodes are needed to fundamentally characterize the silicon wires without individual optimization for the galvanic embedding of the Si wires into a Cu current collector for each wire length and thickness. For the production of paste anodes, the Si microwires are scratched from the bulk Si substrate and mixed with conductive carbon black (1:1 ratio) and CMC and water. The amount of water in these samples is not critical for the electrode preparation nor the performance. The amount of water is only 2 µl. Additional heating under vacuum atmosphere is evaporating the water. EDX measurements show no significant amount of oxide growth on the samples. A thin layer of mixed Si wires is casted on top of a Cu foil, and the produced samples are dried in vacuum at 75°C for 7 h. The Cu foil acts as current collector. During optimization steps, it was ensured that the adhesion between the current collector and the paste is good and does not delaminate during the electrochemical tests. These paste electrodes are used to facilitate the characterization of the wires themselves when lithiated or delithiated in half cells. Figure 2a shows an example of SEM micrograph of a paste electrode. Each wire is surrounded by carbon black, representing conductive paths from the current collector to the Si wires.

To investigate the impact of the thickness and length of the wires on their electrochemical and structural behavior during cycling, wires with five different thicknesses and five different lengths were fabricated for this study (thicknesses ranging from 1.8 to 1.2 µm with a fixed length of 60 µm, and different length from 36 to 75 µm at a thickness of 1.4 µm). The scale-invariant etching technique makes this definite size modulation possible.

Anodes of Wire Arrays

In comparison to paste electrodes where the wires are mixed with conductive additives and casted on a Cu foil, in this approach as wire arrays, the current collector is deposited on top of the array. The wire arrays benefit of their high amount of active material without any carbon due to their mechanical integration and stability to the Cu layer.

In comparison to chemical or physical vapor deposition steps where the adhesion between metal and Si as well as the thickness of the metallic layer has to be improved, the current collector is also deposited purely galvanically. In a first step, a several nm thin Cu seed layer is deposited on top of the Si wires by dissolving Si and reducing the Cu ions. The thickness of the resulting Cu layer after the galvanic

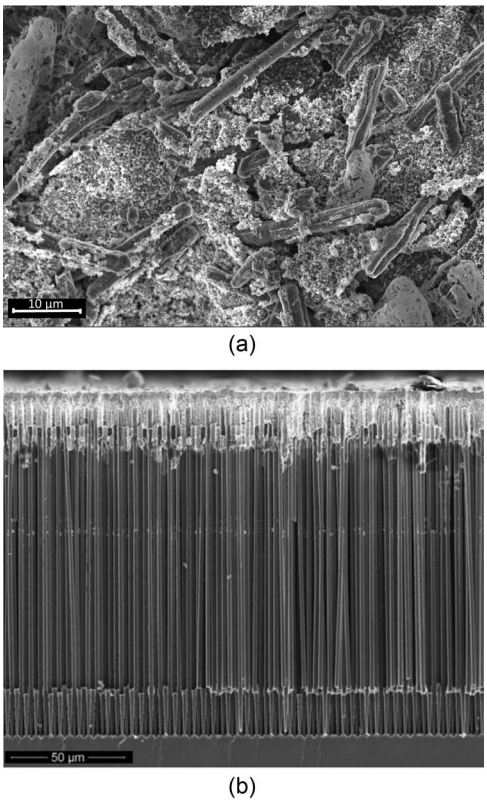

Figure 2. Examples of SEM micrographs of Si microwire anodess a) microwires embedded in a conducting matrix as paste anodes, b) Si wire array with a current collector deposited at its top.

deposition is around 50 µm. There is Cu deposition also between the interstices of the wires, enabling a good mechanical contact. The wire tips of 5 to 10 µm are fixed in this Cu layer. Due to the mechanical stability of the embedded wires, it is possible to detach the whole array from the substrate (with the current collector). A deliberate change in the current-time profile during the electrochemical etching of the macorpores (refer to "processing of the microwires") at the pore tips allows the easy detachment from the substrate.[1] This concept of Si anode is the the only one used for performance tests.

Experiments showed that this mechanical integration of the wires into the current collector is a key parameter of the good cyclability. During cycling, the wires expand when Li-ions incorporate into the wires, leaving the fixed part of the silicon "uncharged" – there is no alloy formation in the bottom part of the wires.

Not only the electrochemical and/or chemical etching steps are scale invariant, but also the deposition of the current collector is no longer limited to small areas. To overcome large potential differences across larger areas of the Si wafer (during deposition), small nucleation centers of Cu are created which are embedded in a polymer matrix (EP 14 184 103.1). Around those nucleation points, the Cu grows homogeneously until the nuclei agglomerate and form a homogeneous Cu layer. The polymer matrix can be doped with additional chemistry previously used in the seed layer deposition which makes this separate step unnecessary. The time for the Cu deposition can be reduced in this step up to 50% (5 h).

Electrochemical Characterization

The electrochemical characterization is performed in half cells which are prepared with metallic Li as counter electrode and with the electrolyte LP 30. LP 30 is a standard battery electrolyte provided by BASF, which contains an equal amount of ethylencarbonate (EC) and dimethylcarbonate (DMC) with $LiPF_6$ as Li salt. The half cells

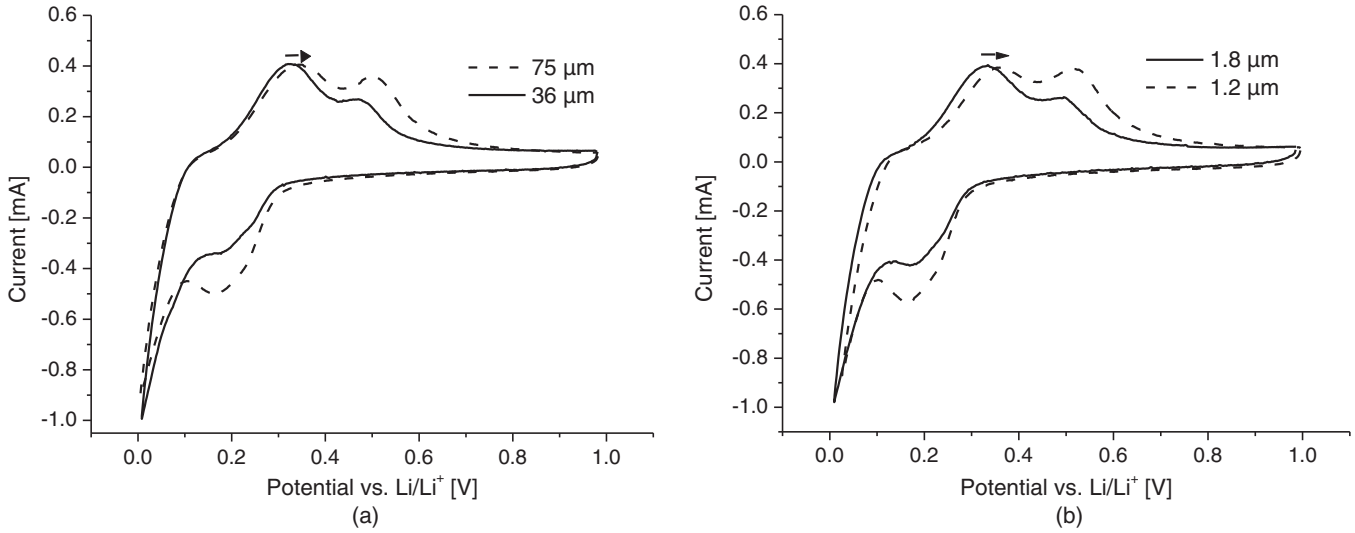

Figure 3. Typical voltammograms for different wire geometries, embedded in paste anodes: a) comparison between two lengths at a constant thickness of 1.4 µm, b) comparison between two thicknesses at a length of 60 µm.

of Si wires are characterized by cyclic voltammetry to investigate the dependency of the potential on the thickness and length of the wires. Both the paste electrodes as well as the wire arrays are tested in half cells. For the voltammetric analysis and the fundamental investigation of the potential shifts with FFT-IS, paste electrodes are used.

FFT-IS was performed in the frequency range of 5 Hz to 20 kHz, using a small signal of 50 mV. Measurements were performed in-operando every minute. During voltammetry measurements, a (potential) scan is applied reversibly between 1 V and 20 mV for five cycles. Phase transformations can be identified in the form of peaks in the voltammograms. The phase transformations are step-wise lithiation and delithiation of Si with Li-ions, which depend on external and internal parameters during a voltammogram.[17,18] Figure 3 shows voltammograms (cycle 3) of Si wires embedded in the paste electrodes with two wire lengths and two thicknesses. The shape of the voltammogram is typical for Si anodes and varies only in the peak positions.[17,19–21]

Figure 3a shows voltammograms of anodes with wires of two different lengths and constant thickness of 1.4 µm. The voltammograms of Figure 3b are from anodes with wires with different thickness with a constant length of 60 µm. The voltammogram's peaks represent phase transformations and are fully reversible indicated by two peaks during the lithiation (from 1 V to 20 mV) and delithiation (from 20 mV to 1 V, reversal of the potential scan). Li ions are incorporated into the silicon wires in a two-step process forming Li_xSi_y alloys undergoing structural (phase) transformations from crystalline to amorphous upon cycling. A fully lithiation peak, represented in Figure 3a and b, is at the potential where the Li-ions are fully incorporated and Li_xSi_y alloys are formed. If the Li-ions are removed from the anode completely, the fully delithiation peak is formed. The partial lithiation as well as delithiation peaks are formed in between the conversion from (crystalline) Si to Si-Li alloys and vice versa. The peak shifts with the size variation are illustrated in Figures 3a and 3b. The peak shift (here only displayed in detail for the partial delithiation peak) is seen in every peak. The lithiation voltage increases almost linearly with the wire length indicating the longer paths for the Li ions or the electrons.

A series resistance model can explain the peak shift in the lithiation voltage, where the different particular series resistances of every wire in the anode contribute to the "average resistance". It is clear that the electronic paths are different for each wire, because of the connectivity to the conductive additive (carbon black), but the average path, translated in an average resistance, depends on the dimensions of the wires. If the wires are longer, the average resistance is larger. Therefore, the increase in the lithiation voltage for longer wires corresponds to higher average resistances inside the wires.[17] Figure 3b indicates the impact of different thicknesses. A comparison between the peak maxima for different thicknesses indicates smaller lithiation and delithiation voltages for thick wires. The average resistance varies with the cross section of the wires, which is consequently larger with thin wires.

The amplitude of the peaks itself is not useful for the examination of the size dependency, since by the given sweep rate (0.1 mV/s) the wires do not get totally lithiated/delithiated. Nevertheless, the width of the peaks provides some information. The partial delithiation peak (first reduction peak) for thin wires, 1.2 µm, is broad in comparison to the thick wires. To explain these results, two components have to be considered. First, faradaic and non-faradaic currents which superimpose the current signal. The only interesting currents are the faradaic currents resulting from the phase transformations. If the sweep rate is too high, the influence and the superposition of both currents are too high and the peaks change their shape from e.g. broad to narrow peaks. The time for the incorporation is faster and lots of irreversible reactions take place. Due to the enhanced sweep rate, the mass transfer is enhanced. The broad peak, mentioned for thin wires, could be explained with a slow(er) lithiation/delithiation process for thin wires.[22–26] A previous study revealed by a comparison of different thicknesses/lengths, that thick wires of 1.8 µm need less incorporations voltages for the lithiation/delithiation than thin wires. These results could be explained by the inverse proportionality of the resistance to the wire area. If the lithiation/delithiation process is easier e.g. less voltage is needed for the incorporation, the mass transfer reaction is enhanced and faster, therefore the peaks are narrower.[25]

Figure 4 shows a schematic of the equivalent circuit used to model the data obtained by FFT impedance spectroscopy.

The equivalent circuit model consists of three RC elements (resistances in parallel to capacitances) in series and an additional series resistance. The series resistance refers to the ohmic losses due to the electrolyte, contacts, and electronic transport through the electrodes. The three parallel resistances namely R_1 to R_3 are referred to as described in the text: R_1 relates to the SEI formation, R_2 relates to the charge transfer into the wires and R_3 originates from the (elastic) interaction of the matrix with the active material. In the schematic, it can be seen that the wires are embedded in the conductive carbon black material in the paste. The equivalent circuit used for our IS-modelling is based on the all our previous studies of composition and structure, and fits very well the measured data. Other models, such those including Warburg impedances are not suitable for us,

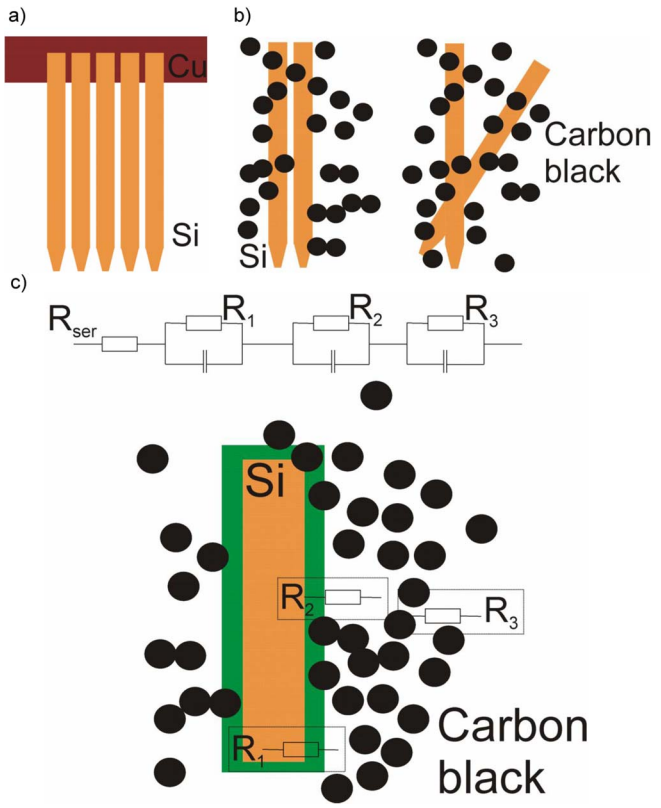

Figure 4. Schematic and equivalent circuit model of the silicon microwires: a) silicon microwire arrays, b) microwires embedded in a paste, c) schematic representation of the three parallel resistances.

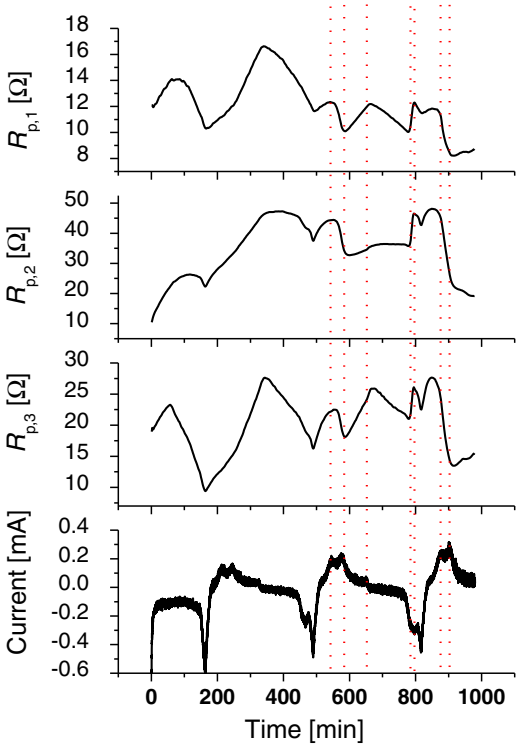

Figure 5. Resistances from FFT-impedance analysis for a wire thickness of 1.8 μm, embedded in paste anodes.

since the slowest frequencies used in the present study (necessary for in-operando FFT-IS) are of 5 Hz, too fast for observing diffusion phenomena.

In the following, the impedance data is discussed in more detail, explaining how the resistances could be related to physical or chemical processes inside the battery anode.

FFT-impedance analysis was performed over three cycles on thick wires (1.8 μm). Figure 5 shows the comparison between the three resistances computed from the measurements, and the recorded current. The electrochemical processes can be modeled with three RC circuits in series. The simultaneous application of DC and AC signals allows to model fast and slow processes on the same sample at the same time. By combining cyclic voltammetry and FFT-impedance spectroscopy, not only the interaction between the paste electrode ingredients can be modelled and the correlation between the formation of the SEI around the wires can be understood as well.

Figure 5 indicates the different behavior of the resistances. $R_{p,1}$ is in the same order of magnitude as the other resistances but slightly smaller while the other two resistances are similar in their values. By comparing the behavior of $R_{p,1}$ on the time scale, the values change in the first cycle while the change of behavior stabilizes in the continuing cycles (almost constant in the last cycles – not presented in this work). This resistance may be related to the SEI,[22,27,28] which forms during the first cycles.

$R_{p,2}$ on the other hand exhibits the highest value during the cycling. This behavior can be directly correlated to the charge transfer into the silicon wires. Obviously for thicker wires the resistance increases, which is in good accordance to the more active material which has to be penetrated and the more bonds which have to be broken when Li ions diffuse into the Si wires, considering that the incorporation of Li ions is mainly radial. Figure 5 presents the resistances $R_{p,1}$ and $R_{p,3}$ and their coupled capacitances, of wires of two different lengths (the ones of Figure 3b). Direct comparison indicates the complementary behavior between both the capacitances and resistances. While $R_{p,1}$ decreases over time, $R_{p,3}$ increases over time (see Figure 6b). On the other hand, the capacitances vary about two orders of magnitude. Due to the direct correlation between the area and the capacitance, thick wires may have a reduced surface to volume ratio (smaller interface to the electrolyte) and show smaller capacitance in comparison to thin wires. Nevertheless, $R_{p,3}$ can most probably be correlated to the (elastic) interaction between the wires and the surrounding matrix containing carbon black. During the large volume expansion, the wires breathe, contracting the conducting material around the wires and producing voids. With longer cycling time, the voids around the wires need longer time to be filled again and the electrolyte has the chance to interact with the paste directly limiting the battery performance.

During the breathing of thick wires, less voids or paths for the electrolyte are formed due to the limited space in the matrix leading to the connection from the cyclic voltammograms and the potential dependency. With increasing wire thickness, $R_{p,3}$ increases (consequently, the capacitance decreases) and a second maxima appears (which is more pronounced in thinner wires). At 560 min (compare Figures 5 and 6b, indicated with a straight line), the system is between both delithiating peaks (conversion between the partial and fully delithiation peaks – removing Li-ions and conversion from Li_xSi_y alloys into pure Si). During this conversion, larger volume expansion occurs, leading to higher resistances (and higher energy which has to be provided) because of the increase in surface area.

In order to compare both wire concepts and distinguish the differences of the diffusional processes inside these anodes, FFT-impedance spectroscopy was also performed for wire arrays which allows a direct comparison of the time constants in both the paste anodes as well as in the wires array anodes. Whereas in paste electrodes the SEI is formed and probably damaged due to its direct contact with the conductive material during the breathing while cycling, in wire arrays the SEI is formed homogeneously from top to the bottom, and is stable over hundreds of cycles. Results of the last variant are shown in Figure 7. The equivalent circuit is also composed of three *RC* circuits in series for which three major time constants are modelled and correlated in Figure 6. It shows the impedance data of one cycle, indicating

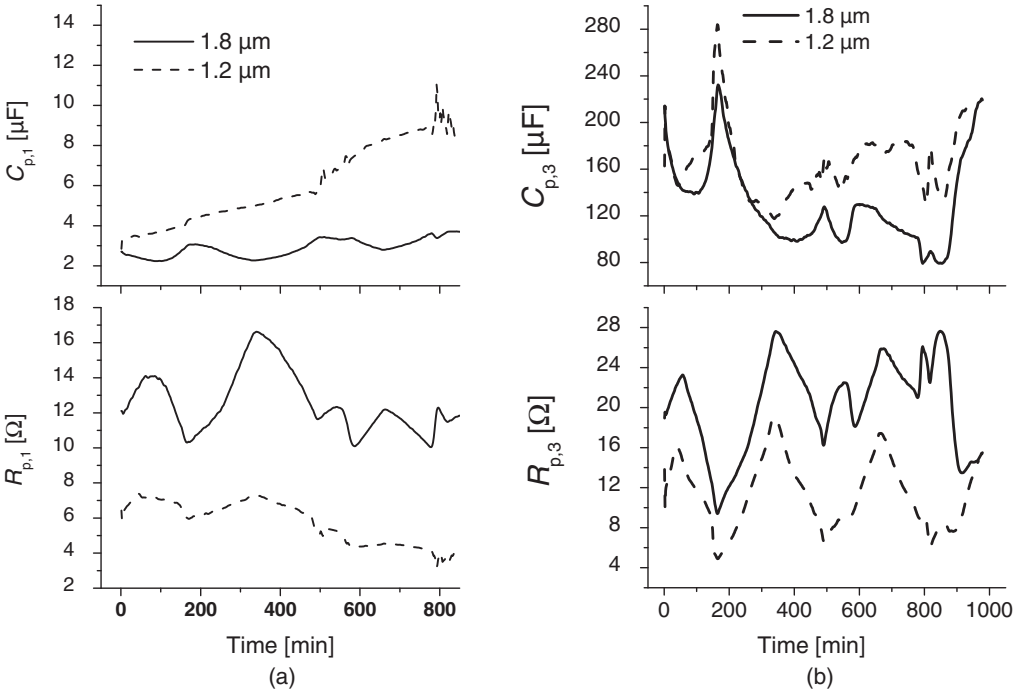

Figure 6. Comparison of resistances for thick wires embedded in paste anodes a) $R_{p,1}$ and $C_{p,1}$ b) $R_{p,3}$ and $C_{p,3}$.

constant voltage and current regions. The cycling is performed with a combination of galvanostatic and potentiostatic steps[12,29] under current and capacity limitations. The slowest time constant τ_3 represents the charge transfer to the Si wires. The other two time constants, whose behavior and order of magnitude are similar, represent the conduction through the electrolyte (τ_1) and through the SEI (τ_2).

The maxima in the slowest time constant τ_3 can be directly correlated to the inflection points in the second derivative of the voltammogram. Those inflection points can be correlated to the phase transformations occurring in Si.[12] By directly comparing the values obtained from the FFT analysis for paste anodes and array anodes, the time constants differ about three orders of magnitudes. This behavior can be explained by the way of connecting the wires to the current collector. Paste anodes, where the Si wires are mixed with conducting carbon black, provide easier connectivity of the active material. This is ellucidated by the faster time constants (RC products of Figures 5, 6 and 7). Nevertheless, due to the interaction between the additives and the Si wires during breathing, the battery performance is hindered. The volume expansion during lithiation/delithiation processes leads to void formation around the wires (loss of contact to the current collector). For the wire arrays (see Figure 1b), the wires are fixed from one side to the current collector and can only expand in one direction. Although the time constants are faster in paste anodes, the battery performance could be optimized and the problems can be indicated due to the simultaneous FFT-impedance analysis.

The FFT-impedance spectroscopy is a powerful tool to indicate battery performance processes which can be used to change fabrication processes, leading to higher (battery) efficiencies.

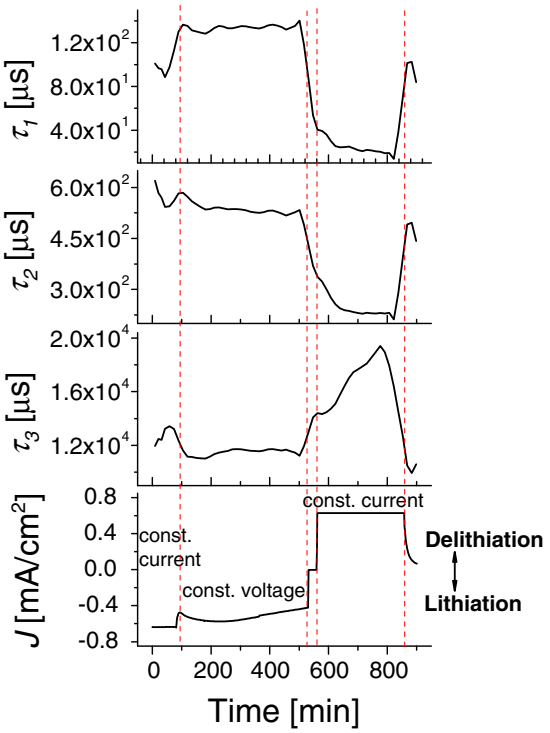

Figure 7. Time constants from FFT-impedance analysis for wire array anode.[1]

Battery Performance

Silicon microwire arrays exhibit a stable capacity of about 3150 mAh/g over 300 cycles. Studies have shown[1,29] that a capacity limitation to 75% of the nominal capacity and a relatively slow cycling rate of *C*/10 are necessary to allow stable SEI formation in the first cycles without any dendrite or crack formation (as happened if cycled to the full capacity). After the first four cycles, the cycling rate is increased to *C*/2.[29] Figure 8a indicates the battery performance under these conditions for the wire arrays. These wires are 70 µm long with a thickness of 1.2 µm. Those wire arrays have an active mass loading of 1.35 mg/cm^2. There is no additional material, except for the current collector. Therefore, the active loading is very high compared to other silicon anodes.

The half cells are tested in half battery cells by a combination of potentiostatic and galvanostatic steps with either current or the capacity limitations are reached. In this case, the capacity limitation is the 75% of the nominal capacity. The voltage limits for these experiments

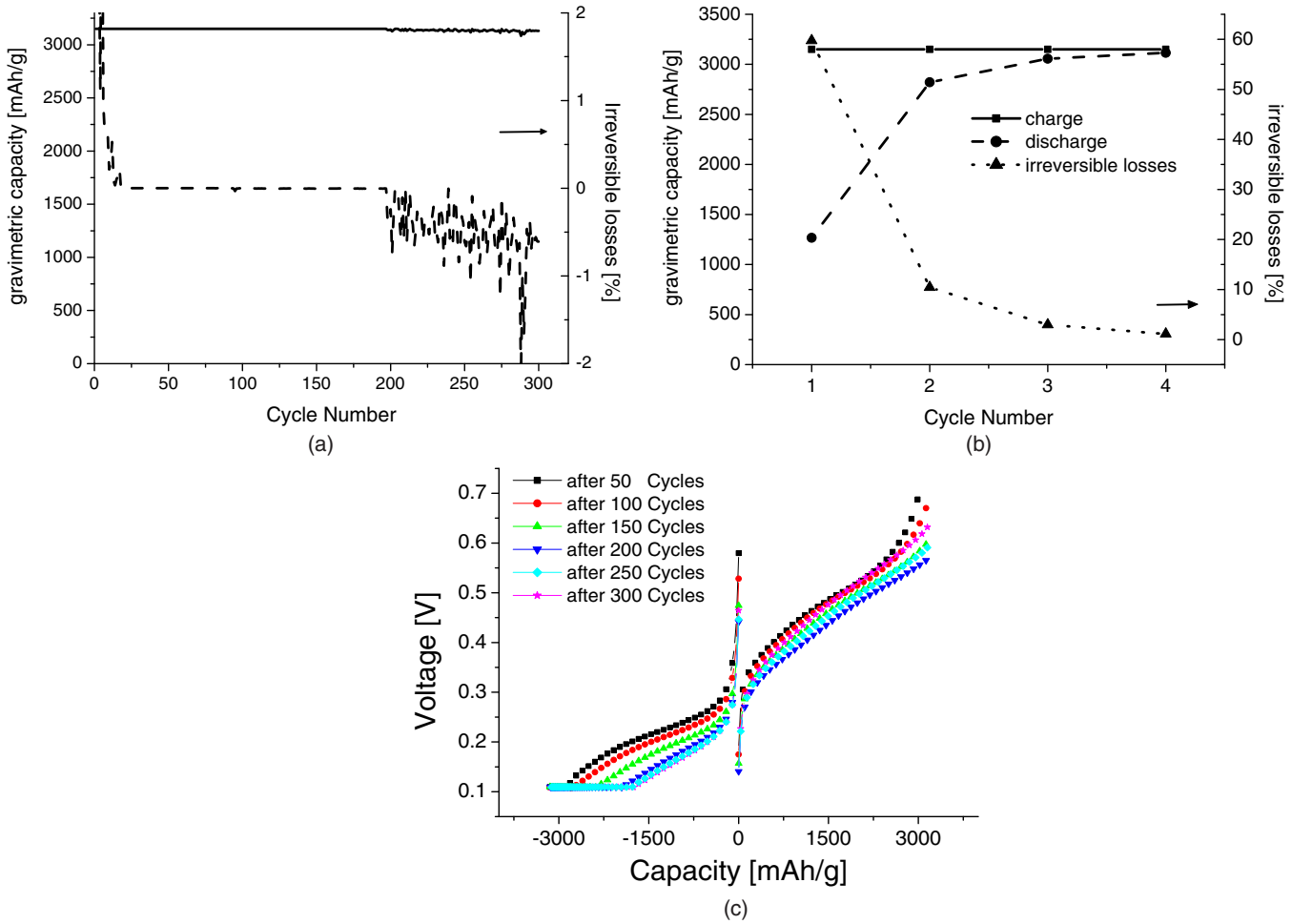

Figure 8. Battery performance with a capacity limitation of 75% SOC for silicon microwire arrays with a length of 70 μm and a thickness of 1.2 μm a) for 300 cycles, b) 5 cycles to demonstrate the irreversible losses occurring in the first three cycles, c) capacity curves depending on the incorporation voltage for every 50 cycles.

are 110 mV and 700 mV. Hundreds of samples were tested under this conditions, and all of them exhibited about the same cycling performances. It has been found that this way of testing is optimal.[12] Optimizations have been lately made (not part of this work) by coating the samples with an additional copper layer to enhance their conductivity and at the same time reduce the series resistance losses.

Figure 8b shows the first charging/discharging cycles. Here, the comparison between the lithiation/delithiation curves and the irreversible losses indicate that the wires only suffer from losses in the first couple of cycles due to the formation of the SEI. The irreversible losses occurring during the first cycles are given by SEI formation. An indication that SEI forms just once, remaining relatively stable during cycling, is the capacity loss approaching to zero after the first charge/discharge cycles. It is known from our previous reports on this kind of microwire-anodes that the SEI layer can be as thick as 250 nm,[1] needing a substantial amount of lithium to be formed; increasing the thickness of this layer at least by 10% would be observed in the capacity vs cycle number curves. Additionally, it has been previously observed in cyclic voltammograms that there is an irreversible peak at 1.17 V appearing just (visibly) during the first lithiation of the Si wires.[29] This irreversible process correlates well with the irreversible loss occurring mainly during the first charge/discharge cycle (SEI formation). On the other hand, XRD, TEM and SEM measurements (which are not shown in this paper) show the same results. The SEI forms homogeneously along every wire but its width does not increase upon cycling after the first 3 cycles. These results are emphasized by the impedance data for both the wire arrays and the paste electrodes. $R_{p,1}$ shows the slowest values and τ_1 is the fastest time constant which is constant and decreases once the formation is finished. Figure 8c shows the (incorporation) voltage depending on the capacity for 50 cycles. It can be observed that the potentiostatic step during lithiation is longer at advanced number of cycles. This implies that with increasing number of cycles, more voltage is needed for the incorporation/formation of the Li_xSi_y. Higher voltages can be also interpreted as higher ohmic losses with larger number of cycles.

The negative irreversible losses appearing over 200 cycles represent non-faradaic currents present when delithiating the wires. This occurs due to conductive paths given by Li dendrites (the counting electrode is Li metal).

Conclusions

This paper presented a scale invariant production technique of Si microwires, which can be used successfully as anodes for Li-ion batteries. Due to the way of fabrication, Si wires with defined thicknesses and lengths can be prepared. They can be modelled and characterized in either paste electrodes with the addition of conducting additives or as arrays with the mechanical stability of a current collector. It has been shown a unique way of characterizing, combining standard cyclic voltammetry with FFT-impedance spectroscopy to obtain distinct information about the influence of the geometries of the anodes and composing Si microwires on the battery parameters. The potential dependency on the thickness and the length in the paste electrodes could be mainly correlated to the ohmic resistances of the wires.

Acknowledgments

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