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# Comparison of light emitting capacitors with textured and polished silicon substrates towards the understanding of the emission mechanisms

J. Alarcón-Salazar[a,*], M.A. Vásquez-Agustín[b], E. Quiroga-González[c], I.E. Zaldívar-Huerta[a], M. Aceves-Mijares[a]

[a] Electronics department, Instituto Nacional de Astrofísica Óptica y Electrónica, Puebla 72000, Mexico
[b] Facultad de Ciencias de la Electrónica, Benemérita Universidad Autónoma de Puebla, Puebla 72570, Mexico
[c] Institute of Physics, Benemérita Universidad Autónoma de Puebla, 72570 Puebla, Mexico

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ABSTRACT

We experimentally compare the optical and electrical characteristics of Light Emitting Capacitors (LECs) using textured and polished silicon surface. The goal of this work is focused to investigate the influence of the roughening of the surface of the silicon substrates in the electro-optical properties of LECs fabricated with off-stoichiometric silicon oxide ($SiO_x$). The textured surface is produced by reactive ion etching using Ar and $SF_6$ as ion sources. It exhibits an average roughness of 4.0 ± 0.2 nm, with a spike density of 3.7 ± 1.8 × $10^{10}$ $cm^{-2}$. The $SiO_x$ is deposited by low-pressure chemical vapor deposition on polished and textured substrates. The turn-on electric field of LECs using textured substrate is reduced from 8.5 MV/cm to 7.0 MV/cm, and the power conversion is improved 4.1 times compared with LECs with polished substrate. Furthermore, in LECs fabricated over textured substrates, the electrical current value increases at low voltages and once it reaches the high current regime, this value remains constant. Then, the spikes on the silicon substrate improve carrier injection towards the $SiO_x$ at low electric fields, causing more trapping of electrons in the $SiO_x$ and enhancing the electroluminescence response at high electric fields. An explanation of the enhanced electro-emission mechanisms is given. Also, a figure of merit that allows the comparison with LECs with different technological characteristics is proposed.

## 1. Introduction

Since the discovery of light emission in porous silicon [1], many efforts have been focused on finding efficient light sources compatible with the Si technology. Several research groups have been investigating Si-compatible light emitting materials and structures, such as Si nanocrystals, Si pn junctions, and off-stoichiometric silicon oxide also named silicon rich oxide (SRO) [2–6]. Thanks to its optical and electrical characteristics, SRO is one of the most promising materials [7–9]. SRO is a multiphase material composed of Si, $SiO_x$ with $0 < x < 2$, and $SiO_2$ [10] that can be obtained by Low-Pressure Chemical Vapor Deposition (LPCVD), Plasma-Enhanced Chemical Vapor Deposition (PECVD), ion implantation, and sputtering [2,10–17].

Specifically, for SRO obtained by LPCVD the Si excess in the films is controlled during the deposition process by the ratio of the precursor gasses (Ro): nitrous oxide and silane [7,10,11]. Ro = 3, Ro = 30 and Ro > 100 produce SRO films with 16, 5, and 0 at% of silicon excess respectively. SRO with Si excesses in the range of 3–14 at% and annealed at 1100 °C in $N_2$ radiates in the range of 400–850 nm under different stimulus [7,9,14,18]. SRO with Si excess in the order of 5% exhibits the highest emission, attributed principally to defects in the films as was demonstrated in [19].

SRO films have been used to fabricate LECs electrically excited. In these devices, SRO is used as the active layer; meanwhile, a transparent polysilicon or Transparent Conductive Oxide (TCO) film (e.g. Indium Tin Oxide, ITO) is deposited instead of a metal gate [12,20]. However, such LECs have the limitation of presenting high turn-on voltage that is near to the dielectric breakdown, making the device unreliable. To solve this issue, the use of multilayer structures of SRO films instead of single layers is a good alternative [12]. Also, it has been demonstrated that LECs fabricated on textured silicon substrates present enhanced electrical and optical characteristics compared with those prepared on polished substrates [12,13,20–22]. The practical use of carrier injection enhanced by tip structures in LECs compatible with CMOS technology is relatively recent. One of the first approaches was addressed in 2007 [20], and since then not much advance has been reported. In this last

* Corresponding author.
*E-mail addresses:* j.alarcon.sal@gmail.com (J. Alarcón-Salazar), maceves@ieee.org (M. Aceves-Mijares).

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reference, the influence of Si nano-pyramids on the current of LEC was studied. The Si nano-pyramids were formed on the surface of a silicon substrate during PECVD deposition of SRO with high Si excess. It was demonstrated that a larger density of nano-pyramids causes that the Fowler-Nordheim (F-N) tunneling threshold takes place at 1.4 MV/cm instead of 7 MV/cm of a LEC with a smooth surface. This is, the nanostructured surface allows a reduction of the voltage needed to turn-on light emission, as a consequence, the breakdown of the dielectric is avoided. Another proposed option is to use SRO doped with rare earth elements (e.g. Erbium) rather than plain SRO [23]; unfortunately, this makes the fabrication more complicated and incompatible with CMOS technology. Using textured silicon substrates seems to be an adequate option to reduce the turn-on voltage. Thus, it is important to explore the effects of different textured substrates on the electroluminescence of SRO-based LECs, especially considering that the number of references about this topic is very limited, as mentioned before. It is important to underline that rough silicon surfaces can be obtained with different techniques, and each technique produces specific LEC´s characteristics.

In this paper, we report a thorough study of the electrical and light-emitting characteristics of LECs on silicon substrates with two different surface characteristics: polished and textured. The textured surfaces were obtained by Reactive Ion Etching (RIE). The main goal of this work, is demonstrate that textured substrates substantially improve the LECs' performance compared with the polished ones. Using textured substrates, the turn-on voltage and the probability of dielectric breakdown in the device are reduced.

## 2. Experimental procedure

LECs were fabricated on single-side-polished ⟨100⟩ p-type Si substrates of resistivity 3.25–6.75 Ω-cm. The RCA cleaning was used throughout the process. The surface of some substrates were textured using RIE during one minute with 7 sccm of Ar and 3 sccm of $SF_6$, and a power of 300 W. In the following, LEC structures with polished substrates will be referred as sample A, and the ones textured substrates as sample B. The fabrication process was as follows: A film of SRO with $R_0 = 30$ ($SRO_{30}$) was deposited by LPCVD at 736 ºC on both substrates. Afterwards, both samples were annealed at 1100 ºC in $N_2$ ambient for 180 min to activate the emission of the SRO films. To complete the LEC structure, a semitransparent polycrystalline Si (Poly) layer was deposited on top and doped n + . Then, lithography was used to form poly gates with area of $1.54 \pm 0.01 \times 10^{-2}$ $cm^2$. Multiple devices were fabricated per Si wafer. Some samples were left without Poly for PL measurements. Subsequently, an Aluminum film 0.6 µm thick was evaporated on the backside of the substrate. Finally, samples were annealed at 460 ºC in forming gas as the final step. The scheme of the fabricated devices is shown in Fig. 1.

The thickness and refractive index of SRO films were measured with a Gaertner L117 null ellipsometer with a He-Ne laser of 632.8 nm. PL spectra were measured with a Horiba Jobin Yvon spectrometer model Fluoro-Max3 with a xenon lamp as light source and a photomultiplier as detector. Samples were excited with UV radiation (300 nm), and the luminescence response was recorded from 370 to 1000 nm with 1 nm resolution. Various optical filters were used to guarantee the excitation wavelength and remove harmonic effects. Surface roughness was analyzed with a Nanosurf easyScan Atomic Force microscope (AFM). The analyzed area was 5 µm x 5 µm in non-contact mode. Scanning Electron Microscope (SEM) observations were performed utilizing an Ultra Plus SEM from Zeiss. Current versus voltage (I-V) and Capacitance versus voltage (C-V) measurements were obtained with a Keithley source-meter model 2400 and a Keithley semiconductor parameter analyzer model 4200-SCS, respectively. To obtain the EL spectra, the Keithley source-meter was used to apply the excitation voltages and the Fluoro-Max3 spectrometer was used to record the emitted light. The optical power from the emitted light was measured with a 1400 IL radiometer connected to an UV–VIS GaAsP detector placed in front of the gate of the samples. To be able to compare the EL intensity of the different samples, all measurements were done consecutively the same day and with the same experimental setup. Several devices of the same kind were tested to assure reproducibility.

## 3. Results and analysis

### 3.1. Substrate characteristics

Fig. 2(a) and (b) are FM images corresponding to the surface of the substrates for sample A (polished) and B (textured). The surface of sample B shows spikes of conical shape with a spike density of $3.7 \pm 1.8 \times 10^{10}$ $cm^{-2}$, and 4.0 ± 0.2 nm average roughness. For sample A the average roughness is 0.5 nm. Fig. 2(c) is a SEM photomicrograph that confirms the conical features of the textured sample.

Table 1 summarizes the values of thickness and refractive index of the luminescent SRO layer for both samples after annealing. The thickness difference between films is around 4%, which is ascribed to the fabrication technique. It is well know that variations as big as 10% could be obtained, even within the same wafer [24,25], for LPCVD films.

### 3.2. Photoluminescence

Fig. 3 shows normalized PL spectra for samples A and B. It is notorious that the shape of the PL spectra for both samples is identical, indicating that the PL is independent of the morphology of the Si surface. The emission spectra consist of two broad bands (peaks). The first and most intense peak is centered at 1.72 eV (722 nm), whereas the second one is centered at 2.90 eV (428 nm) (inset of Fig. 3). These bands will be named hereafter as "red" and "blue" bands, respectively. The present results agree with previous reports on the PL of $SRO_{30}$ [14,19].

Fig. 4(a) illustrates a deconvolution of the PL red band in three

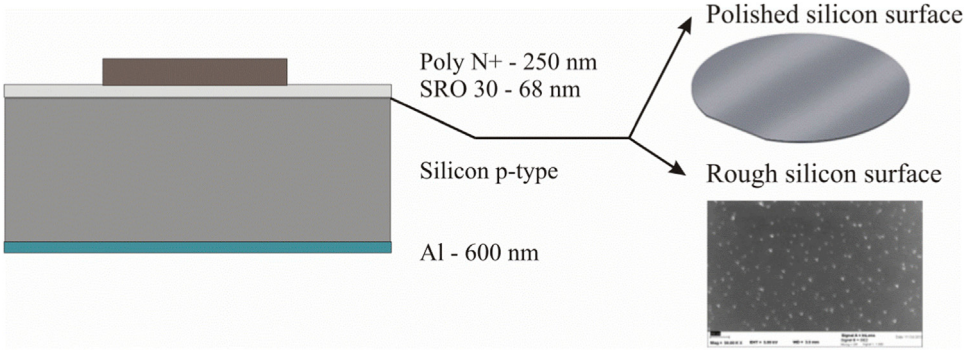


**Fig. 1.** Scheme depicting the components of the fabricated LECs.

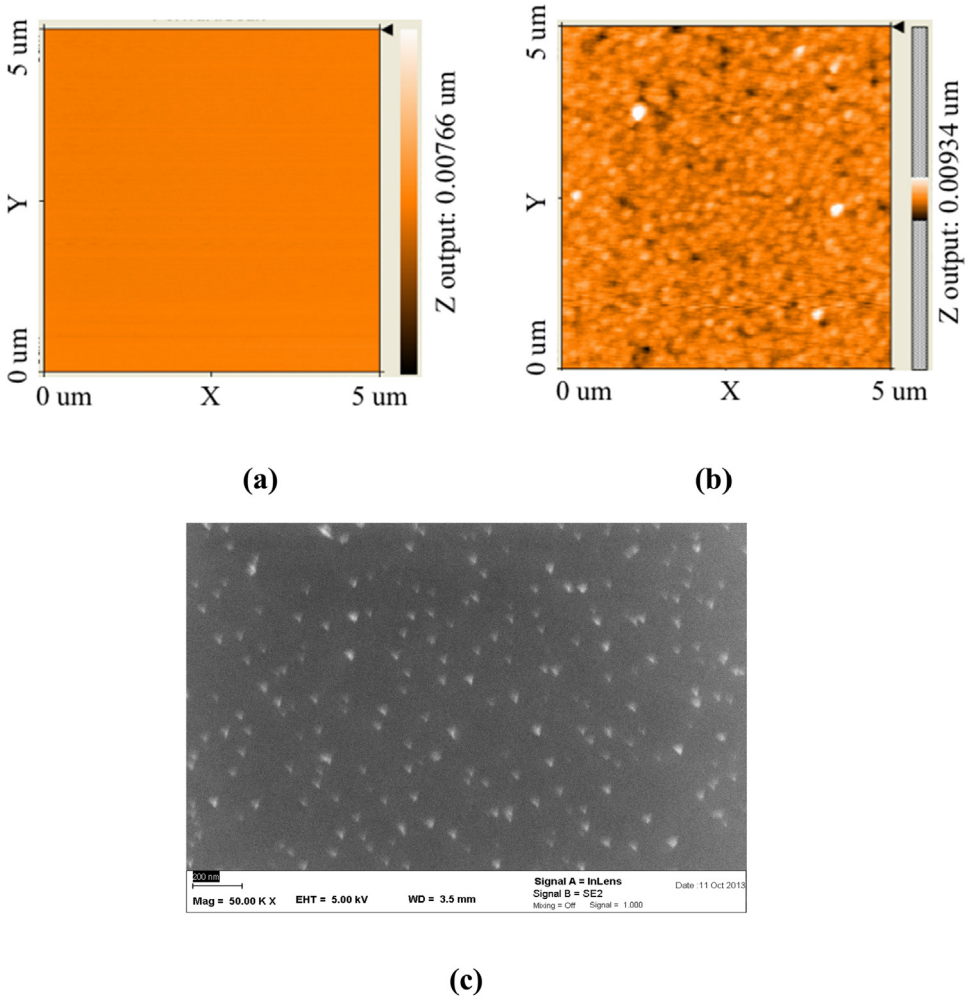


**Fig. 2.** Micrographs of the substrate's surface of the samples. (a) AFM micrograph of a polished substrate; (b) AFM micrograph of a textured substrate; (c) SEM micrograph of a textured substrate.

**Table 1**
Average thickness and refractive index of annealed $SRO_{30}$ film for both samples.

| Sample | Thickness [nm] | Refractive index |
|---|---|---|
| **A** | 65.9 ± 0.4 | 1.51 ± 0.01 |
| **B** | 68.8 ± 1.7 | 1.53 ± 0.01 |

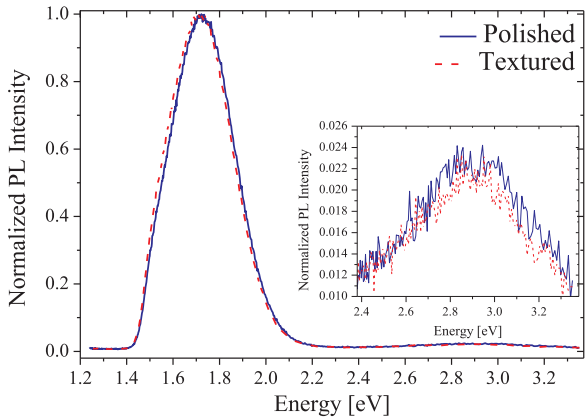


**Fig. 3.** Normalized PL spectra of samples with polished and textured silicon surface. The red band centered at 1.72 eV (722 nm) is the most intense. The inset shows the blue band, centered at 2.9 eV (428 nm).

components centered at 1.55, 1.69 and 1.8 eV. The Peak centered at 1.55 eV can be attributed to interfacial defects at Si nanocluster boundaries with the silicon oxide matrix, as was reported in [18]. Peaks located at 1.69 and 1.8 eV could be related to defects in the oxide matrix, as oxygen vacancies caused by the excess of Si [10,14,19]. Fig. 4(b) shows the deconvolution of the PL blue band in two peaks centered at 2.62 and 2.91 eV. These peaks can be associated to non-bridging oxygen, as was reported in [26].

### 3.3. Electrical characteristics

Fig. 5 shows representative C-V curves for both LECs (several devices at different points of the wafers were measured). These results are used to estimate the dielectric constant and the trap density. The dielectric constant ($K_{SRO}$) is computed as:

$$K_{SRO} = \frac{C_{\max} t_{SRO}}{A\varepsilon_0} \tag{1}$$

where $C_{max}$ corresponds to the maximum capacitance obtained from the C-V curve, $t_{SRO}$ is the thickness of SRO layer, $A$ is the gate area, and $\varepsilon_0$ is the dielectric permittivity of vacuum. The density per unit area and per volume ($Q_t$ and $N_t$, respectively) are calculated as:

$$Q_t = \frac{C_{\max} \Delta V}{Aq} \tag{2}$$

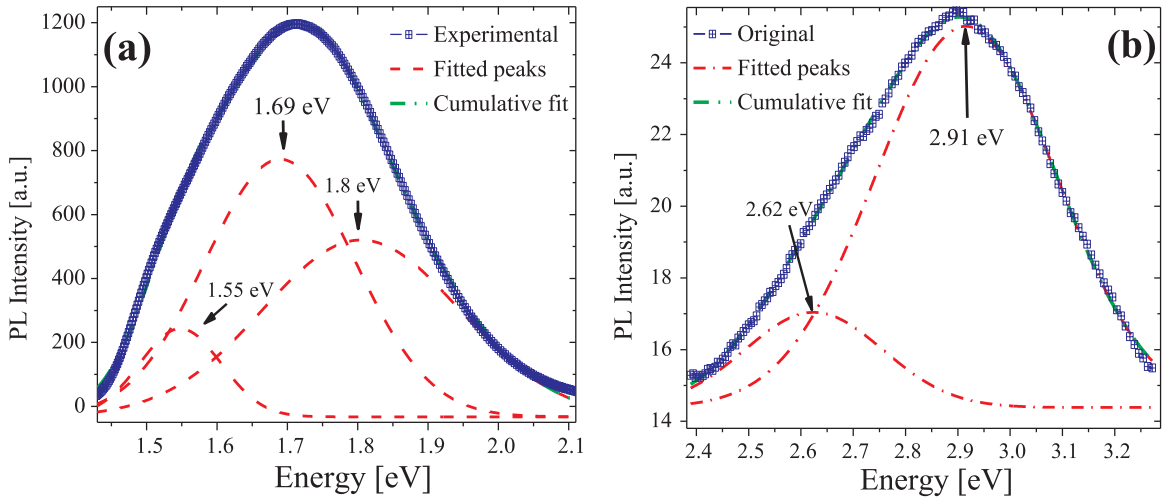


**Fig. 4.** Deconvoluted PL spectra of (a) red band and (b) blue band.

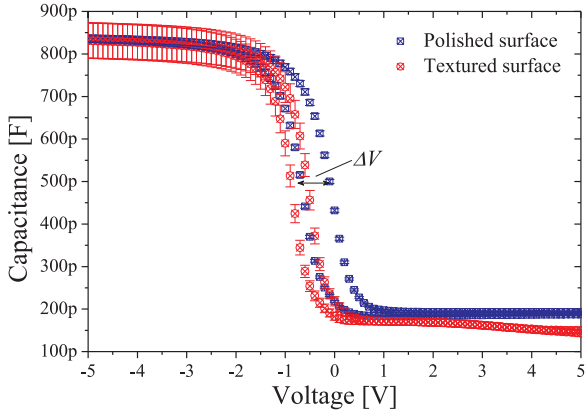


**Fig. 5.** C-V curves for LECs with textured and polished silicon surface.

$$N_t = \frac{Q_t}{t_{SRO}} \tag{3}$$

being $q$ the electron charge, and $\Delta V$ the voltage shift, as shown in Fig. 5. The estimated values of dielectric constant for samples A and B are 4.07 ± 0.02 and 4.22 ± 0.11, respectively. It is clear that given the variation of values, the material is practically the same in both cases. The values are in good agreement with the ones reported in [8].

Table 2 summarizes the parameters obtained from C-V measurements. The trapped charge density per area and volume is 21% and 24% lower in sample B. This could be attributed to the enhancement of the electron transport in this sample due to the textured surface, as will be seen in the I-V curves.

Fig. 6 displays the average I-V curves for both LECs, and their variation. These curves show the typical behavior of a MOS capacitor using SRO instead of $SiO_2$ [7]. It is notorious that sample B achieves higher currents at moderate voltages. For example, at 10 V a current difference of one order of magnitude between sample A ($\sim 10^{-8}$ A) and B ($\sim 10^{-7}$ A) is observed.

Fig. 7(a) shows the current density ($J$) as function of the electric field ($E$) when a positive voltage with respect to the substrate is applied to the gate (condition to obtain EL). In this figure, three regions are marked for the analysis of the electrical behavior of the LECs: region I corresponds at low electric fields (0–1.5 MV/cm), region II at moderate electric fields (2–5 MV/cm) and region III at high electric fields (> 5 MV/cm).

At low electric fields, charge transport is dominated by Ohmic conduction. In this case, the current density as a function of electric field is defined as [27]:

$$J = \sigma \cdot E \tag{4}$$

where $\sigma$ is the conductivity. As can be observed in Fig. 7(b), the LEC with polished substrate exhibits a linear dependence between $J$ and $E$, as expected. However, in sample B, an exponential growth is observed, probably caused by the carrier injection to SRO30. As samples A and B have the same amount of radiative defects (as confirmed by PL) and the same dielectric characteristics (as inferred from C-V measurements), the exponential behavior of the $J$-$E$ curve at low $E$ in sample B must be ascribed to the silicon surface roughening and not to changes in the SRO (carrier injection and not carrier transport).

At moderate electric fields (see Fig. 7(c)), the charge transport is due to Fowler-Nordheim (FN) tunneling mechanism [27] for both samples. The J-E curves of both samples can be fitted with the following equation [28]:

$$J = \frac{C_1 \gamma E^2}{\phi} \exp\left(-\frac{C_2 \phi^{3/2}}{\gamma E}\right) \tag{5}$$

where $C_1$ and $C_2$ are constants, $\varphi$ is the work function and $\gamma$ is named field-enhancement factor [28].

At high electric fields (≥ 5 MV/cm), the Trap-Assisted Tunneling (TAT) mechanism dominates the conduction in both samples. Fig. 8 shows $ln\, J$ vs $1/E$ curves of A and B samples; the solid lines are the fitted curves with the TAT model. The TAT mechanism defines the current density as [27]:

$$J_{TAT} \propto \left(-\frac{8\pi\sqrt{2qm^*}\phi_t^{3/2}}{3hE}\right) \tag{6}$$

where $m^*$ is the electron effective mass, $h$ is the Planck constant and $\phi_t$

**Table 2**
Parameters obtained from the C-V curves for both samples.

| Sample | $C_{max}$ [pF] | $C_{min}$ [pF] | $K_{SRO}$ | $C_{FB}$ [pF] | $\Delta V_{FB}$ [V] | $Q_t$ [traps cm$^{-2}$] | $N_t$ [traps cm$^{-3}$] |
|---|---|---|---|---|---|---|---|
| A | 841.6 | 192.98 | 4.07 ± 0.02 | 703.1 | 0.87 | $2.96 \times 10^{11}$ | $4.50 \times 10^{16}$ |
| B | 836.3 | 171.07 | 4.22 ± 0.19 | 697.3 | 0.69 | $2.34 \times 10^{11}$ | $3.40 \times 10^{16}$ |

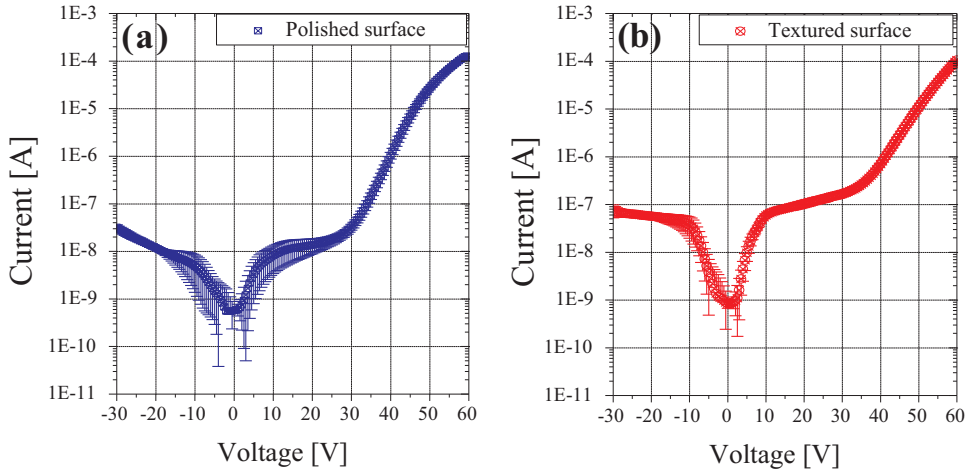


**Fig. 6.** I-V curves for LEC structures of (a) polished sample A and (b) textured sample B, the bars show the variation between different devices.

is the trap level.

As can been seen, both samples have similar *ln J* vs *1/E* curves. Trap levels ($\phi_t$) of 1.49 eV and 1.55 eV were estimated for samples A and B respectively. As expected, practically both values are the same. It is important to remark that under this high *E* regime EL is obtained for both samples.

Both samples have the same conduction mechanisms. The only difference, as can be seen in Fig. 7, is that at low voltages the current in sample B increases faster than in sample A. The current excess is maintained up to the beginning of the high electric field, and at particular high field, the current of the polished sample overlaps to that of the textured one.

Fig. 9 displays an idealized schematic of the conduction trajectories in both samples. When positive voltages are applied to the gate with respect to the substrate, electrons start to move from the substrate towards the gate. At low electric fields, some electrons are injected from

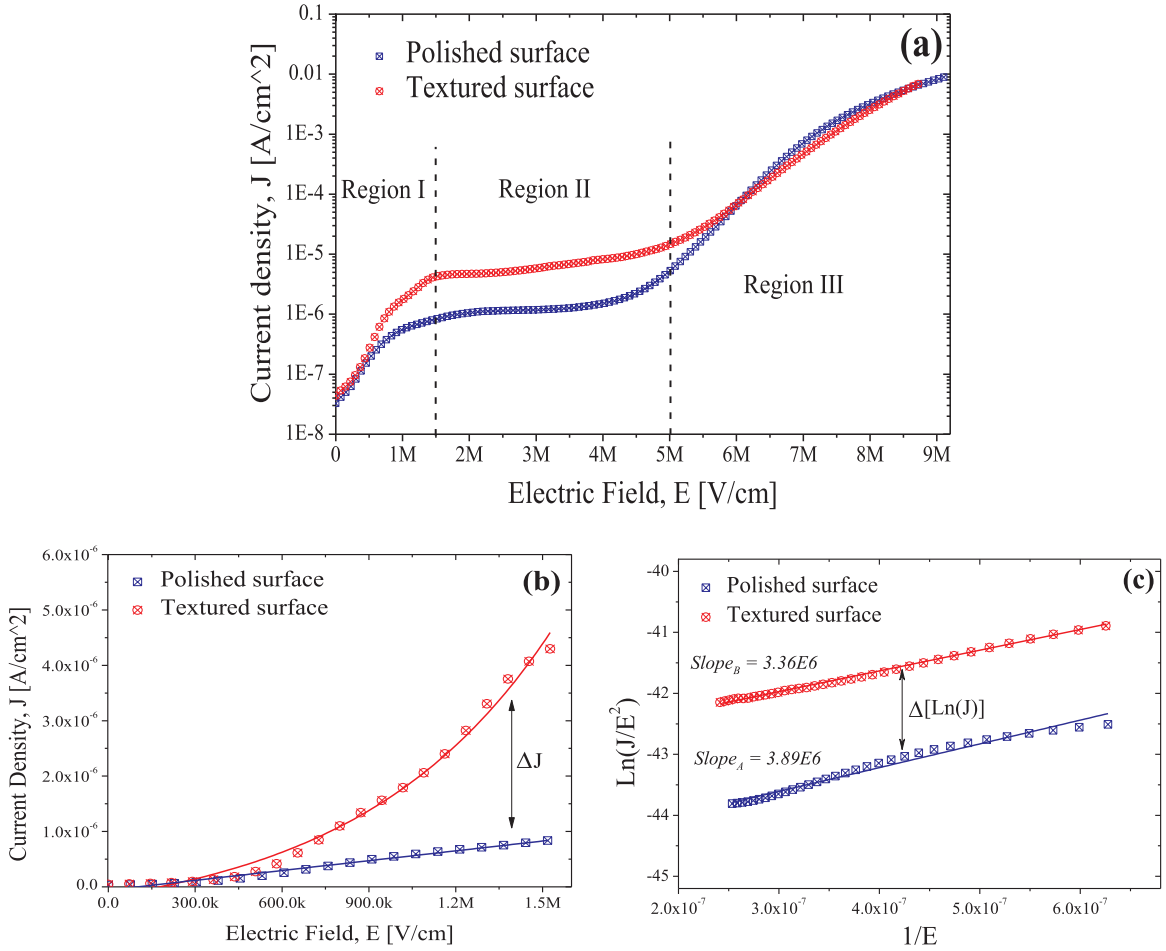


**Fig. 7.** (a) Semi-logarithmic *J-E* curves obtained under forward bias for sample A and B. (b) *J-E* at low electric fields and (c) Fowler-Nordheim plots at moderate electric fields.

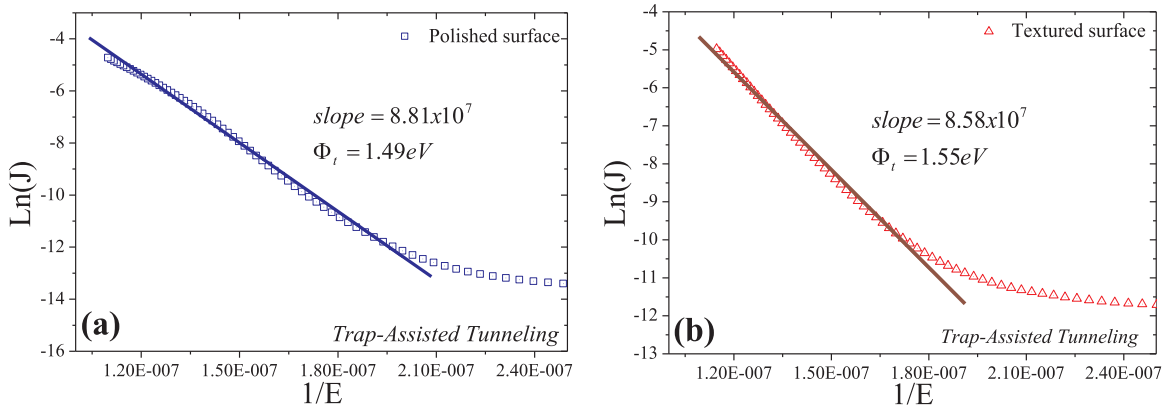


**Fig. 8.** Trap-Assisted Tunneling plot for LECs with (a) polished and (b) textured Si substrates.

Si towards the $SRO_{30}$, and they are able to move across ohmic paths produced by defect levels. Because $SRO_{30}$ is rich in Si-O defects where electrons can move, a chain of such defects can produce such trajectories; for example, the path *i* shown in Fig. 9(a). These defect levels present low activation energies, thus low energy is required to free electrons from these levels. These trajectories are the preferential paths at low fields. However, some electrons are trapped by another kind of defects (indicated as black dots inside gray circles in Fig. 9) that act like "traps", and they require higher energies to release electrons (path *ii* in Fig. 9). Therefore, some barriers are formed, forcing new-coming electrons to move to a different low energy trajectory (path *iii* in Fig. 9). When LECs are built using a polished Si substrate, a low number of preferential paths are used from the many possible, due to the small number of electrons available at the silicon surface. However, when LECs are fabricated using a textured substrate, as the electric field is enhanced in sharp tips, the density of electrons increases at these points; thus, carrier injection is enhanced at the tips, increasing the probability for electrons to move through multiple low resistive paths, as observed in Fig. 9(b). As a consequence, the current density in sample B increases exponentially at low electric fields compared with that of sample A, as shown in Fig. 7(b). From this figure, a current improvement factor (ratio of currents) of approximately 5 can be obtained at 1.5 MV/cm.

At moderate electric fields, as was previously discussed, the FN tunneling mechanism governs the charge transport. This means that the trapped electrons must surmount FN barriers, and then electrons tunnel towards free defect sites (path *iv* in Fig. 9(a)). As LEC with textured substrate initially generates more electrons moving over preferential paths, a higher FN current density is observed in sample B compared with sample A. However, as was observed in Fig. 7(c), both samples have comparable slopes, indicating that similar energies are required to tunnel electrons across the FN barriers.

From the FN plots ($\ln(J/E^2)$ vs $1/E$) shown in Fig. 7(c), and using Eq. (5), the slope is:

$$m = -\frac{C_2\phi^{3/2}}{\gamma} \tag{7}$$

As already demonstrated, the $SRO_{30}$ film common to both samples, preserves its characteristics independently of the Si substrate surface. Then, it is possible to assume that $\phi$ has the same value for both samples, thus $C_2\phi^{3/2}$ is a constant with the same value for samples A and B. Therefore, it is possible to relate both slopes:

$$m_A\gamma_A = m_B\gamma_B \tag{8}$$

where the subscripts A and B refer to samples A and B. Slope values of $3.89 \times 10^6$ and $3.36 \times 10^6$ $[(\mathrm{Vcm}^{-1})^*\ln(\mathrm{AV}^{-1})]$ were determined for sample A and B respectively, from Fig. 7(c). Thus, the field-enhancement ratio is:

$$\frac{\gamma_B}{\gamma_A} = \frac{m_A}{m_B} = 1.15 \tag{9}$$

Because of $\gamma_B$ and $\gamma_A$ are basically the same; the rate of current growth for both samples is practically identical (equal slopes). According to this, the FN gain of sample B with respect to sample A is negligible. This is in contrast to the conclusions presented in [28], where the authors suggest that in a substrate with field-emitters (textured), there is a current gain as compared with polished substrates. In the present case, the results suggest that the current difference is due to the electron injection enhancement at low electric fields in the textured sample.

In the high field regime, electrons are trapped in high-energy traps blocking out the conduction paths. The blockade produces that electrons accumulate forming electron clusters or "clouds"; therefore, electrons have to jump between trajectories as shown in Fig. 9(b), causing that TAT dominates over other conduction mechanisms. A

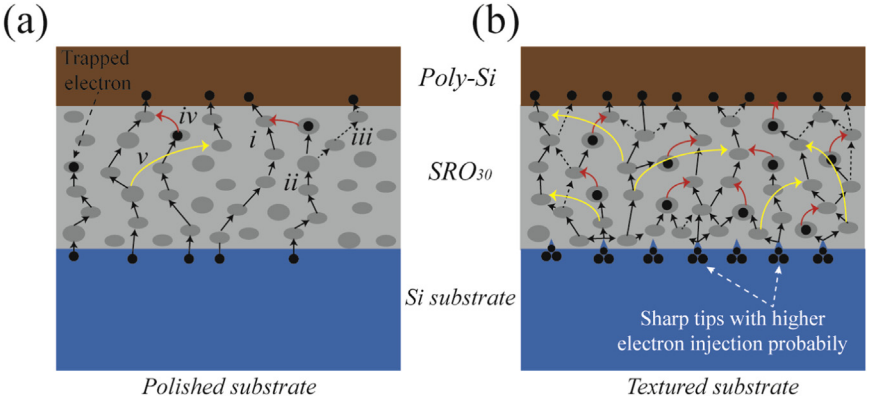


**Fig. 9.** Idealized scheme of the conductive trajectories for LECs with (a) polished and (b) textured Si substrates. Black points indicate electrons trapped that require higher energy to be released. Path *i* is of electrons moving through low energetic traps (preferential paths). Path *ii* is a trajectory finishing in a trapped electron. Path *iii* is an alternative trajectory for electrons arriving at a filled trap. Path *iv* indicates that trapped electrons move through FN from one trap to another at moderate electric fields. Path *v* shows a process presented in the high electric field regimen when electrons tunnel between trap sites (TAT mechanism) and could recombine producing light emission (EL is observed).

higher density of conduction paths is used when the surface of the substrate is textured. In polished substrates, the same phenomenon occurs but through less conduction paths.

It is important to mention that light emission is observable in the LECs with naked eye in the high electric fields. In literature, there are reports indicating that in silicon oxide with a high density of defects TAT conduction and recombination are present simultaneously at high electric fields [7,11,29,30]. In SRO, there are a lot of positive and negative charged defects; therefore, it is plausible that in the present samples both mechanisms take place. From the high population of highly energetic electrons moving by TAT in SRO, some of them recombine emitting photons or not. As the electric field increases, the density of electrons increases and the emission probability increases. This process is schematized as path *v* in Fig. 9, where some electrons could decay between defects producing radiative recombination.

For the first time, it is shown that tips on the substrate could increase the electronic density in transit through SRO when polarizing the LECs, and that this high population increases the probability of light emission at lower voltages.

### 3.4. Electro-optical characteristics

Electroluminescence arises when the gate is positively polarized with respect to the p-type substrate. Under this condition, an n-type inversion layer is formed underneath the silicon surface injecting electrons through the SRO film. As was reported in [12,20], and inferred from the previous section, at high electric fields these electrons are responsible for the radiative recombination in SRO-related defects. Fig. 10 shows the EL spectra of LECs with polished and textured substrates. It is evident that sample B shows a substantial improvement in EL intensity of at least twice with regard to sample A. The polarization voltage was selected to obtain the highest emission for each device: sample A was polarized with 80 V and the current was 113 μA, and sample B with 65 V and the current was 54.5 μA.

Fig. 11 (a) and (b) show the components of the EL spectra for samples A and B respectively. Because both spectra are similar, the same emissive components are observed. Comparing these spectra with the ones of Fig. 4, it can be observed that the peaks centered at 1.55, 1.69, 1.8, 2.62 and 2.91 eV are observed in both, PL and EL; thus the same emissive centers are responsible for both kinds of emission. However, a new peak at 2.09 eV is found in EL. This peak has been related to silicon dangling bonds defects in $SiO_x$ [32] and it has been found in the EL spectra of multilayered structures of SRO [29]. Then, PL and EL have the same origin, and in general all emission mechanisms are related to SRO-related defects. However, in EL the blue and red bands have similar intensities, while in PL the major peak is the red

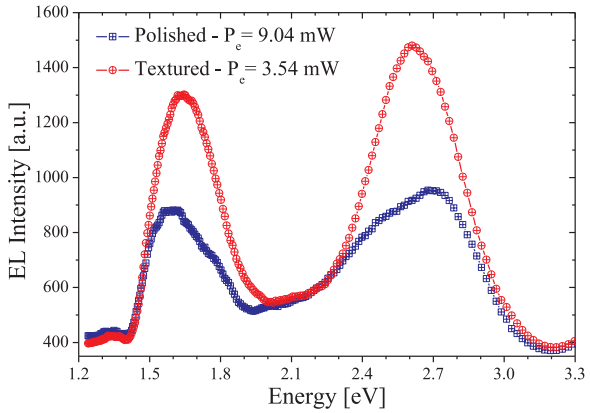


**Fig. 10.** EL spectra of LECs with polished and textured Si substrate. The electrical power applied to the textured LEC is 2.6 times lower than that applied to the polished substrate, and in spite of this, its light emission is almost the double.

one. The EL blue peak is produced by high energy electrons, while in PL low energetic photons produce the red band. The fact that EL produces intense blue emission agrees with the argument that electrons are forced to decay from higher energy levels to find low resistive trajectories, as explained above. This has been also corroborated in cathodeluminescence studies where very energetic electrons produce a high blue emission [14].

The proportion of peak contributions to the total luminescence (area below the curve) is approximately the same for both samples. Just the peak widths change, being narrower for sample B. It can be inferred that the textured substrates have a focusing effect, reducing dispersion: the emitting centers with activation energies closer to the center of the peaks are the most likely to emit in textured samples, since the electronic transport is enhanced and the average trapping time is reduced.

Fig. 12 displays the integrated EL intensity as function of the electric field. As can be seen, EL intensity depends linearly of the electric field. Sample B turns-on the EL at an electric field of 7 MV/cm; meanwhile, sample A requires an electric field of 8.5 MV/cm. This demonstrates that a reduction of the turn-on electric field is achieved roughening the Si substrate. To compare both LECs, a linear fitting was carried out. The slope of the curve for sample B is higher than for sample A. The slope ratio between samples (B/A) is 4.5, thus the EL intensity of sample B increases 4.5 times faster than that of sample A.

The power conversion ratio ($\eta_c$) is defined as:

$$\eta_c = \frac{P_{op}}{P_e} \tag{10}$$

where $P_{op}$ is the optical power emitted by the LEC and $P_e$ is the electrical power consumed during the emission. In the devices of this report, the electrical power (Pe) to obtain the highest EL intensity was 9.04 mW and 3.54 mW for samples A and B, respectively. The measured optical power of sample A and B were 0.17 μW and 0.27 μW, correspondingly. This indicates that LEC with textured Si substrate consumes 2.6 times less electrical power and emits 60% higher optical power than the LEC with polished substrate. As a consequence, the power conversion ratio is $18.8 \times 10^{-6}$ ($1.8 \times 10^{-3}$ %) and $76.2 \times 10^{-6}$ ($7.6 \times 10^{-3}$ %) for samples A and B, respectively. Therefore, the LEC with textured substrate improves 4.1 times the power conversion with regard to the LEC with polished substrate. These values agree well with those reported in the literature [4,31]. The points where the electric field is the same for both samples are enclosed in a dashed rectangle in Fig. 12, clearly showing that the textured sample presents enhanced electrical and optical characteristics.

In spite of the low power conversion, it was already demonstrated that the LEC emission is enough to be used in practical devices [4]. Nonetheless, the most important characteristic of LECs with textured substrates is that their working voltages are low enough to avoid electrical damage.

It is difficult to compare the characteristics of the LECs of the present work with the LECs reported in literature, since all of them present different dimensions (area of the contacts and thickness of the emissive layer), different gate material, etc. Hence, it is proposed the volumetric electrical power density times the average transmittance of the gate material ($\delta$) as a figure of merit to evaluate LECs:

$$\delta = J_{on} E_{on} T \tag{11}$$

where $J_{on}$ is the current density and $E_{on}$ is the electric field, both measured when whole area emission is reached; $T$ is the average optical transmittance in the wavelength range of the emission. The smaller is $\delta$, the better is the LEC. Consequently, for sample A:

$$\delta_A = \left(6.1 \times 10^{-3} \frac{A}{cm^2}\right)\left(8.5 \times 10^{6} \frac{V}{cm}\right) T = 5.19 \times 10^{4}(T) \frac{VA}{cm^3} \tag{12}$$

and for sample B:

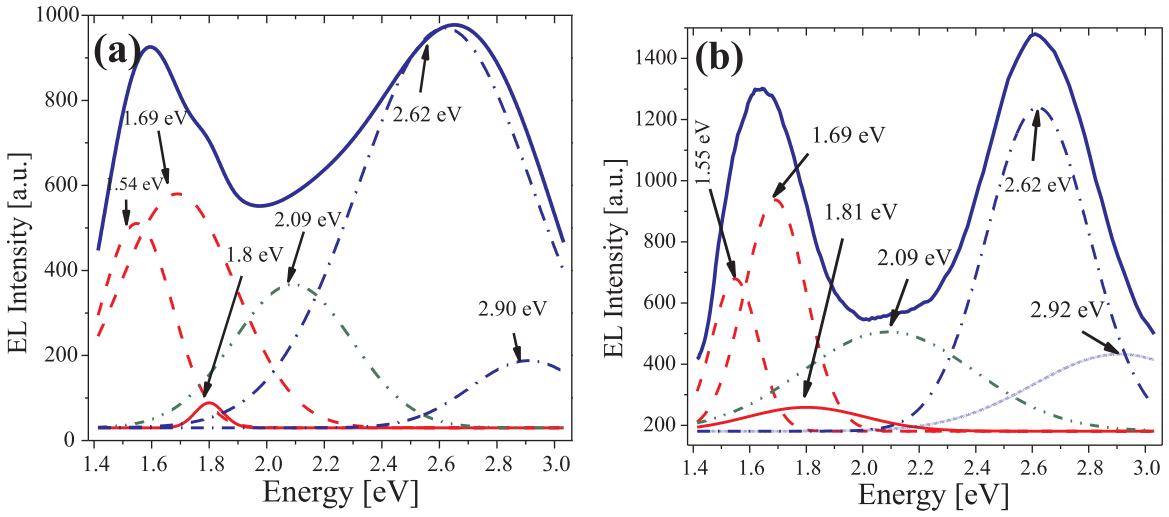


**Fig. 11.** Decomposed EL spectra of LECs with (a) polished and (b) textured surfaces. The experimental spectra are in solid line, dashed and dotted lines represent the fitted peaks.

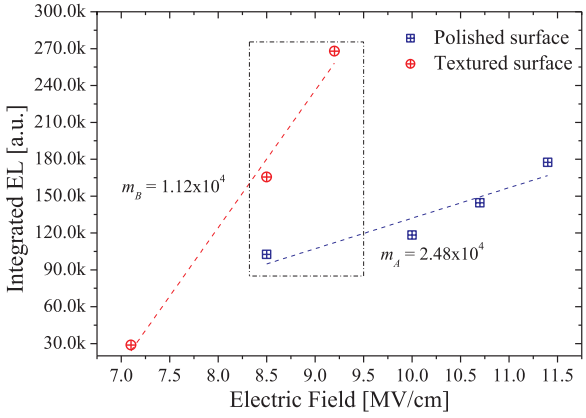


**Fig. 12.** LECs' integrated EL intensity as function of the applied electric field for LECs with polished (sample A) and textured (sample B) substrates. Linear dependence is observed for both samples. The initial EL that is observed with the naked eye arises at 7 MV/cm for sample B, and at 8.5 MV/cm for sample A.

$$\delta_B = \left(3.4 \times 10^{-4} \frac{A}{cm^2}\right)\left(7 \times 10^{6} \frac{V}{cm}\right) T = 2.38 \times 10^{3}(T) \frac{VA}{cm^3} \quad (13)$$

A way to estimate the average transmittance of polysilicon, that is the gate material for our LECs, was reported in [29], where experimental points were linearly fitted and then the average transmittance value was determined from it. LECs A and B have the same gate material; therefore it is not necessary to consider the transmittance to compare between the devices. However, considering a transmittance of 35% obtained at a 650 nm wavelength, $\delta_A$ and $\delta_B$ turn out to be $1.8 \times 10^4$ [VA/cm$^3$] and $8.3 \times 10^2$ [VA/cm$^3$] respectively.

## 4. Conclusion

Two light emitting capacitors (LECs) were fabricated using $SRO_{30}$ as active material: one of them on polished silicon and another one on textured silicon. The textured silicon surface was generated using ion etching. It was observed that the PL spectra are independent of the silicon surface morphology. Also, EL was observed in both samples, and it was determined that PL and EL had the same origin: SRO-related defects. The charge transport mechanisms were analyzed and they point out to be the same for both samples. Ohmic conduction, Fowler-Nordheim tunneling, and Trap-Assisted Tunneling govern the charge transport at low, moderate, and high electric fields, respectively. It was demonstrated that textured silicon surface with density of peaks of $3.7 \times 10^{10}$ cm$^{-2}$ increases 5 times the current density across the $SRO_{30}$ film at low electric fields compared with that of polished surfaces, thus more electrons are injected into the SRO in the textured samples. Texturing the substrate improves the power conversion approximately 4 times. Additionally, there is an enhancement of the injection of electrons, and the EL intensity, while there is a reduction of the turn-on voltage. The whole enhancements have been achieved without modifying the intrinsic characteristics of $SRO_{30}$. This kind of LEC represents another opportunity to solve functionality and reliability of silicon light sources.

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